HARDWARE REFERENCE MANUAL

Turbo PMAC PCI

PC Bus Expansion Board with Piggyback CPU

4xx-603588-xHxx

April 27, 2010

DELTA TAU
Data Systems, Inc.
NEW IDEAS IN MOTION ...

Single Source Machine Control *Power // Flexibility // Ease of Use*
21314 Lassen Street Chatsworth, CA 91311 // Tel. (818) 998-2095 Fax. (818) 998-7807 // www.deltatau.com

Copyright Information

© 2010 Delta Tau Data Systems, Inc. All rights reserved.

This document is furnished for the customers of Delta Tau Data Systems, Inc. Other uses are unauthorized without written permission of Delta Tau Data Systems, Inc. Information contained in this manual may be updated from time-to-time due to product improvements, etc., and may not conform in every respect to former issues.

To report errors or inconsistencies, call or email:

Delta Tau Data Systems, Inc. Technical Support
Phone: (818) 717-5656
Fax: (818) 998-7807
Email: support@deltatau.com
Website: http://www.deltatau.com

Operating Conditions

All Delta Tau Data Systems, Inc. motion controller products, accessories, and amplifiers contain static sensitive components that can be damaged by incorrect handling. When installing or handling Delta Tau Data Systems, Inc. products, avoid contact with highly insulated materials. Only qualified personnel should be allowed to handle this equipment.

In the case of industrial applications, we expect our products to be protected from hazardous or conductive materials and/or environments that could cause harm to the controller by damaging components or causing electrical shorts. When our products are used in an industrial environment, install them into an industrial electrical cabinet or industrial PC to protect them from excessive or corrosive moisture, abnormal ambient temperatures, and conductive materials. If Delta Tau Data Systems, Inc. products are exposed to hazardous or conductive materials and/or environments, we cannot guarantee their operation.

REVISION HISTORY				
REV.	**DESCRIPTION**	**DATE**	**CHG**	**APPVD**
1	UPDATED E-POINT JUMPER DESCRIPTIONS	10/19/06	CP	M. COGUR
2	UPDATED JUMPER SETTINGS FOR E121 & E122	04/27/10	CP	S. SATTARI

Table of Contents

INTRODUCTION **1**
Board Configuration 1
Base Version *1*
Option 1: Additional 4 Channels Axis Interface Circuitry *1*
Option 2: Dual-Ported RAM *1*
Option 2B: High-Speed USB Communications Interface *1*
Option 4: CPU Type *2*
Option 5: CPU and Memory Configurations *2*
Option 7: Plate Mounting *3*
Option 8: High-Accuracy Clock Crystal *3*
Option 9T: Auxiliary Serial Port *3*
Option 10: Firmware Version Specification *3*
Option 12: Analog-to-Digital Converters *3*
Option 15: V-to-F Converter for Analog Input *3*
Option 16: Battery-Backed Parameter Memory *3*
Option 18: Identification Number & Real-Time Clock/Calendar Module *4*
PMAC Connectors and Indicators 4
J1 - Display Port (JDISP Port) *4*
J2 - Control-Panel Port (JPAN Port) *4*
J3 - Thumbwheel Multiplexer Port (JTHW Port) *4*
J4 - Serial Port (JRS422 Port) *4*
J5 - General-Purpose Digital Inputs and Outputs (JOPTO Port) *4*
J6 – Expansion Port (JXIO Port) *4*
J7 / J8 - Machine Connectors (JMACH2/JMACH1 Ports) *4*
J9 – Compare Equal Outputs Port (JEQU Port) *5*
J30 – Optional Analog to Digital Inputs (JANA Port) *5*
J31 – Optional Universal Serial Bus Port (JUSB Port) *5*
JS1 / JS2 – Expansion Ports (JS1 / JS2 Ports) *5*
TB1 – Power Supply Terminal Block (JPWR Connector) *5*
LED Indicators *5*
PMAC Board Layout Part Number 603588-100 6
PMAC Board Dimensions Part Number 603588-100 7

JUMPER SUMMARY **9**
Power-Supply Configuration Jumpers 9
Clock Configuration Jumpers 10
Encoder Configuration Jumpers 10
Board Reset/Save Jumpers 10
Communication Jumpers 10
I/O Configuration Jumpers 11
Reserved Configuration Jumpers 12
Piggyback Turbo CPU Board Jumper Configuration 12
Watchdog Timer Jumper *12*
Dual-Ported RAM Source Jumper *12*
Power-Up State Jumpers *13*
Firmware Load Jumper *13*

CPU BOARD E-POINT DESCRIPTIONS **15**
E1: Watchdog Disable Jumper 15
E2: DPRAM Location Configure 15
E4 – E6: Power-Up/Reset Load Source 15
E7: Firmware Reload Enable 15

MAIN BOARD E-POINT DESCRIPTIONS 17
E0: Machine Output 17
E1 - E2: Machine Output Supply Voltage Configure 17
E3 - E6: Servo Clock Frequency Control 18
E7: Machine Input Source/Sink Control 18
E17A-D: Amplifier Enable/Direction Polarity Control 19
E17E-H: Amplifier Enable/Direction Polarity Control 19
E22 - E23: Control Panel Handwheel Enable 20
E28: Following Error/Watchdog Timer Signal Control 20
E29 - E33: Phase Clock Frequency Control 20
E34 - E38: Encoder Sampling Clock Frequency Control 21
E40 - E43: Software Address Control 21
E48: CPU Clock Frequency Control (Option CPU Section) 22
E49: Serial Communications Parity Control 22
E50: Flash Save Enable/Disable 22
E51: Normal/Re-Initializing Power-Up 22
E54 - E65: Host Interrupt Signal Select 23
E72 - E73: Panel Analog Time Base Signal Enable 24
E74 - E75: Clock Output Control for Ext. Interpolation 24
E85: Host-Supplied Analog Power Source Enable 25
E87 - E88: Host-Supplied Analog Power Source Enable 25
E89: Amplifier-Supplied Switch Pull-Up Enable 25
E90: Host-Supplied Switch Pull-Up Enable 25
E98: DAC/ADC Clock Frequency Control 26
E100: Output Flag Supply Select 26
E101 - E102: Motors 1-4 Amplifier Enable Output Configure 26
E109: Reserved for Future Use 27
E110: Serial Port Configure 27
E111: Clock Lines Output Enable 27
E114 - E115: Motors 5-8 Amplifier Enable Output Configure 27
E121 - E122: XIN Feature Selection 28

MACHINE CONNECTIONS 29
Mounting 29
Power Supplies 29
Digital Power Supply 29
Analog Power Supply 29
Flags Power Supply (Optional) 30
Overtravel Limits and Home Switches 30
Resistor Pack Configuration: Flag and Digital Inputs Voltage Selection 30
Types of Overtravel Limits 30
Home Switches 30
Motor Signals Connections (JMACH Connectors) 31
Resistor Pack Configuration: Termination Resistors 31
Resistor Pack Configuration: Differential or Single-Ended Encoder Selection 31
Incremental Encoder Connection 32
DAC Output Signals 32
Amplifier Enable Signal (AENAx/DIRn) 33
Amplifier Fault Signal (FAULTn) 33
General-Purpose Digital Inputs and Outputs (JOPTO Port) 34
Control-Panel Port I/O (JPAN Port) 34
Command Inputs 35
Selector Inputs 35
Alternate Use 35
Reset Input 35

Handwheel Inputs *35*
Optional Voltage to Frequency Converter *35*
Thumbwheel Multiplexer Port (JTHW Port) 36
Optional Analog Inputs (JANA Port) 36
Compare Equal Outputs Port (JEQU Port) 37
Serial Port (JRS422 Port) 37
Machine Connections Example 38

MATING CONNECTORS 39
Base Board Connectors 39
J1 (JDISP)/Display *39*
J2 (JPAN)/Control Panel *39*
J3 (JTHW)/Multiplexer Port *39*
J4 (JRS422)/RS232 or 422/Serial Communications *39*
J5 (JOPT)/OPTO I/O *39*
J6 (JXIO)/Expansion Board *39*
J7 (JMACH2)/Second Machine Connector (Option 1 Required) *39*
J8 (JMACH1)/First Machine Connector *39*
JS1/A-D Inputs 1-4 ..... *40*
JS2/A-D Inputs 5-8 (Option 1 Required) *40*
JEQU/Position Compare *40*
JANA/Analog Inputs Option *40*
CPU Board Connectors 40
J2 (JEXP)/Expansion *40*
J8 (JAUX232)/Auxiliary RS232 ..... *40*

BASE BOARD CONNECTOR PINOUTS 41
J1: Display Port Connector 41
J2: Control Panel Port Connector 42
J3: Multiplexer Port Connector 43
J4: Serial Port Connector 44
J5: I/O Port Connector 45
J6: Auxiliary I/O Port Connector 46
J7: Machine Port 2 Connector 47
J8: Machine Port 1 Connector 49
J9 (JEQU): Position-Compare Connector 51
J30 (JANA) Analog Input Port Connector (Optional) 51
J31 (JUSB) Universal Serial Bus Port (Optional) 52
JS1: A/D Port 1 Connector 52
JS2: A/D Port 2 Connector 53
TB1 (JPWR) 53

SOFTWARE SETUP 55
Communications 55
PMAC I-Variables 55

INTRODUCTION

The Turbo PMAC PCI is a member of the Turbo PMAC family of boards optimized for interface to traditional servo drives with single analog inputs representing velocity or torque commands. Its software is capable of 32 axes of control. It can have up to eight channels of on-board axis interface circuitry. It can also support up to 32 channels of off-board axis interface circuitry through its expansion port, connected to Acc-24P or Acc-24P2 boards.

The Turbo PMAC PCI is a full-sized PCI-bus expansion card, with a small piggyback board containing the CPU. This piggyback board occupies part of the next slot, but ½-sized boards (such as the Option 2 Dual-Ported RAM board) are also permitted in this next slot. While the Turbo PMAC PCI is capable of PCI bus communications, with or without the optional dual-ported RAM, it does not need to be inserted into a PCI expansion slot. Communications can be done through an RS-232 or RS-422 serial port. Standalone operation is possible.

Board Configuration

Base Version

The base version of the Turbo PMAC PCI provides a 1-1/2-slot board with:

- 80 MHz DSP56303 CPU (120 MHz PMAC equivalent)
- 128k x 24 SRAM compiled/assembled program memory (5C0)
- 128k x 24 SRAM user data memory (5C0)
- 1M x 8 flash memory for user backup & firmware (5C0)
- Latest released firmware version
- RS-232/422 serial interface, PCI (PC) bus interface
- 4 channels axis interface circuitry, each including:
  - 16-bit +/-10V analog output
  - 3-channel differential/single-ended encoder input
  - 4 input flags, 2 output flags
  - Interface to external 16-bit serial ADC
- Display, control panel, muxed I/O, direct I/O interface ports
- PID/notch/feedforward servo algorithms
- Extended "pole-placement" servo algorithms
- 1-year warranty from date of shipment
- One manuals CD per set of one to four PMACs in shipment
  (Cables, mounting plates, mating connectors not included)

Option 1: Additional 4 Channels Axis Interface Circuitry

- Option 1 provides an additional four channels of on-board axis interface circuitry, identical to the standard first four channels.

Option 2: Dual-Ported RAM

Dual-ported RAM provides a very high-speed communications path for bus communications with the host computer through a bank of shared memory. DPRAM is advised if more than 100 data items per second are to be passed between the controller and the host computer in either direction.

- Option 2 provides an 8k x 16 bank of dual-ported RAM on a separate half-slot board.

Option 2B: High-Speed USB Communications Interface

Option-2B provides the high-speed USB communications interface, which is a faster method of communication than the standard RS-232 communications port.

Option 4: CPU Type

The Turbo PMAC PC CPU piggyback board comes standard with a DSP56303 CPU IC as component U1. This CPU has enough internal memory to process the servo and commutation for the first 15 motors. The algorithms for the last 17 motors must be processed from slower external memory. The optional DSP56309 CPU has additional internal memory, so the processing of these motors is significantly improved. The processor type in the board is reported on receipt of the **CPU** command.

- Option 4C: 80 MHz DSP56309 CPU IC. Recommended for control of more than 16 axes, especially with PMAC-based commutation. Not compatible with Options 5Dx.
- Option 4D: 100 MHz DSP56309 CPU IC. Recommended for control of more than 16 axes, especially with PMAC-based commutation. Not compatible with Options 5Cx (including the default Option 5C0.

Option 5: CPU and Memory Configurations

The various versions of Option 5 provide different CPU speeds and main memory sizes on the piggyback CPU board. Only one Option 5xx may be selected for the board.

The CPU is a DSP5630x IC as component U1. It is currently available only as an 80 MHz device (with computational power equivalent to a 120 MHz non-Turbo PMAC).

The compiled/assembled-program memory SRAM ICs are located in U14, U15, and U16. These ICs form the active memory for the firmware, compiled PLCs, and user-written phase/servo algorithms. These can be 128k x 8 ICs (for a 128k x 24 bank), fitting in the smaller footprint, or they can be the larger 512k x 8 ICs (for a 512k x 24 bank), fitting in the full footprint.

The user-data memory SRAM ICs are located in U11, U12, and U13. These ICs form the active memory for user motion programs, uncompiled PLC programs, and user tables and buffers. These can be 128k x 8 ICs (for a 128k x 24 bank), fitting in the smaller footprint, or they can be the larger 512k x 8 ICs (for a 512k x 24 bank), fitting in the full footprint.

The flash memory IC is located in U10. This IC forms the non-volatile memory for the board's firmware, the user setup variables, and for user programs, tables, and buffers. It can be 1M x 8, 2M x 8, or 4M x 8 in capacity.

- Option 5C0 is the standard CPU and memory configuration. It is provided automatically if Option 5xx is not specified. It provides an 80 MHz CPU (120 MHz PMAC equivalent), 128k x24 of compiled/assembled program memory, 128k x 24 of user data memory; and a 1M x 8 flash memory.
- Option 5C1 provides an 80 MHz CPU (120 MHz PMAC equivalent), 128k x 24 of compiled/assembled program memory, an expanded 512k x 24 of user data memory, and a 2M x 8 flash memory.
- Option 5C2 provides an 80 MHz CPU (120 MHz PMAC equivalent), an expanded 512k x 24 of compiled/assembled program memory, 128k x 24 of user data memory, and a 2M x 8 flash memory.
- Option 5C3 provides an 80 MHz CPU (120 MHz PMAC equivalent), an expanded 512k x 24 of compiled/assembled program memory, an expanded 512k x 24 of user data memory, and a 4M x 8 flash memory.
- Option 5D0 provides a 100 MHz CPU (150 MHz PMAC equivalent), 128k x24 of compiled/assembled program memory, 128k x 24 of user data memory; and a 1M x 8 flash memory.
- Option 5D1 provides a 100 MHz CPU (150 MHz PMAC equivalent), 128k x 24 of compiled/assembled program memory, an expanded 512k x 24 of user data memory, and a 2M x 8 flash memory.

- Option 5D2 provides a 100 MHz CPU (150 MHz PMAC equivalent), an expanded 512k x 24 of compiled/assembled program memory, 128k x 24 of user data memory, and a 2M x 8 flash memory.
- Option 5D3 provides a 100 MHz CPU (150 MHz PMAC equivalent), an expanded 512k x 24 of compiled/assembled program memory, an expanded 512k x 24 of user data memory, and a 4M x 8 flash memory.

Option 7: Plate Mounting

Option 7 provides a mounting plate connected to the PMAC with standoffs. It is used to install the PMAC in standalone applications.

Option 8: High-Accuracy Clock Crystal

The Turbo PMAC PC has a clock crystal (component Y1) of nominal frequency 19.6608 MHz (~20 MHz). The standard crystal's accuracy specification is +/-100 ppm.

- Option 8A provides a nominal 19.6608 MHz crystal with a +/-15 ppm accuracy specification.

Option 9T: Auxiliary Serial Port

Option 9T adds an auxiliary RS-232 port on the CPU piggyback board. The key components added are IC U22 and connector J8 on the CPU board.

Option 10: Firmware Version Specification

Normally the Turbo PMAC PC is provided with the newest released firmware version. A label on the U10 flash memory IC shows the firmware version loaded at the factory.

- Option 10 provides for a user-specified firmware version.

Option 12: Analog-to-Digital Converters

- Option 12 permits the installation of 8 or 16 channels of on-board multiplexed analog-to-digital converters. One or two of these converters are read every phase interrupt. The analog inputs are not optically isolated, and each can have a 0 – 5V input range, or a +/-2.5V input range, individually selectable.
- Option 12 provides an 8-channel 12-bit A/D converter. The key components on the board are U20 and connector J30.
- Option 12A provides an additional 8-channel 12-bit A/D converter. The key component on the board is U22.

Option 15: V-to-F Converter for Analog Input

The JPAN control panel port on the Turbo PMAC PC has an optional analog input called Wiper (because it is often tied to a potentiometer's wiper pin). Turbo PMAC PC can digitize this signal by passing it through an optional voltage-to-frequency converter, using E-point jumpers to feed this into the Encoder 4 circuitry (no other use is then permitted), and executing frequency calculations using the time base feature of the encoder conversion table.

- Option 15 provides a voltage-to-frequency converter that permits the use of the Wiper input on the control panel port.

Option 16: Battery-Backed Parameter Memory

The contents of the standard memory are not retained through a power-down or reset unless they have been saved to flash memory first. Option 16 provides supplemental battery-backed RAM for real-time parameter storage that is ideal for holding machine state parameters in case of an unexpected power-down. The battery is located at component BT1.

- Option 16A provides a 32k x 24 bank of battery-backed parameter RAM in components U17, U18, and U19, fitting in the smaller footprint for those locations.
- Option 16B provides a 128k x 24 bank of battery-backed parameter RAM in components U17, U18, and U19, filling the full footprint for those locations.

Option 18: Identification Number & Real-Time Clock/Calendar Module

Option 18 provides a module at location U5 that contains an electronic identification number, and/or a real-time clock/calendar.

- Option 18A provides an electronic identification number module.
- Option 18B provides an electronic identification number module with a real-time clock and calendar. The year representation in the calendar is a 4-digit value.

PMAC Connectors and Indicators

J1 - Display Port (JDISP Port)

The JDISP connector allows connection of the Acc-12 or Acc-12A liquid crystal display, or of the Acc-12C vacuum fluorescent display. Both text and variable values may be shown on these displays through the use of the **DISPLAY** command, executing in either motion or PLC programs.

J2 - Control-Panel Port (JPAN Port)

The JPAN connector is a 26-pin connector with dedicated control inputs, dedicated indicator outputs, a quadrature encoder input, and an analog input (requires PMAC Option 15). The control inputs are low true with internal pull-up resistors. They have predefined functions unless the control-panel-disable I-variable (I2) has been set to 1. If this is the case, they may be used as general-purpose inputs by assigning M-variable to their corresponding memory-map locations (bits of Y address $78800).

J3 - Thumbwheel Multiplexer Port (JTHW Port)

The Thumbwheel Multiplexer Port, or Multiplexer Port, on the JTHW connector has eight input lines and eight output lines. The output lines can be used to multiplex large numbers of inputs and outputs on the port, and Delta Tau provides accessory boards and software structures (special M-variable definitions) to capitalize on this feature. Up to 32 of the multiplexed I/O boards may be daisy-chained on the port, in any combination.

J4 - Serial Port (JRS422 Port)

For serial communications, use a serial cable to connect the PC's COM port to the PMAC's serial port connector. Delta Tau provides the Acc-3D cable for this purpose, which connects PMAC to a DB-25 connector. Standard DB-9-to-DB-25 or DB-25-to-DB-9 adapters may be needed for a particular setup.

J5 - General-Purpose Digital Inputs and Outputs (JOPTO Port)

PMAC's JOPTO connector provides eight general-purpose digital inputs and eight general-purpose digital outputs. Each input and each output has its own corresponding ground pin in the opposite row. The 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules. Delta Tau's Acc-21F is a six-foot cable for this purpose.

J6 – Expansion Port (JXIO Port)

This port is used only when connecting to optional PMAC accessory boards.

J7 / J8 - Machine Connectors (JMACH2/JMACH1 Ports)

The primary machine interface connector is JMACH1, labeled J8 on the PMAC PCI. It contains the pins for four channels of machine I/O: analog outputs, incremental encoder inputs, and associated input and output flags, plus power-supply connections. The next machine interface connector is JMACH2, labeled J7 on the PMAC PCI. It is essentially identical to the JMACH1 connector for one to four more axes. It is present only if the PMAC card has been fully populated to handle eight axes (Option 1), because it interfaces the optional extra components.

J9 – Compare Equal Outputs Port (JEQU Port)

The compare-equals (EQU) outputs have a dedicated use of providing a signal edge when an encoder position reaches a pre-loaded value. This is very useful for scanning and measurement applications. Instructions for use of these outputs are covered in detail in the PMAC User Manual.

J30 – Optional Analog to Digital Inputs (JANA Port)

This optional port is used to bring in the analog signals for the optional analog to digital inputs set. This feature provides up to 16 analog inputs in the range of 0 to 5V unipolar or ±2.5V bipolar.

J31 – Optional Universal Serial Bus Port (JUSB Port)

This optional port allows communicating with PMAC through a standard USB connection.

JS1 / JS2 – Expansion Ports (JS1 / JS2 Ports)

These ports are used only when connecting to optional PMAC accessory boards.

TB1 – Power Supply Terminal Block (JPWR Connector)

This terminal block may be used as an alternative power supply connector if PMAC PCI is not installed in a PCI-bus.

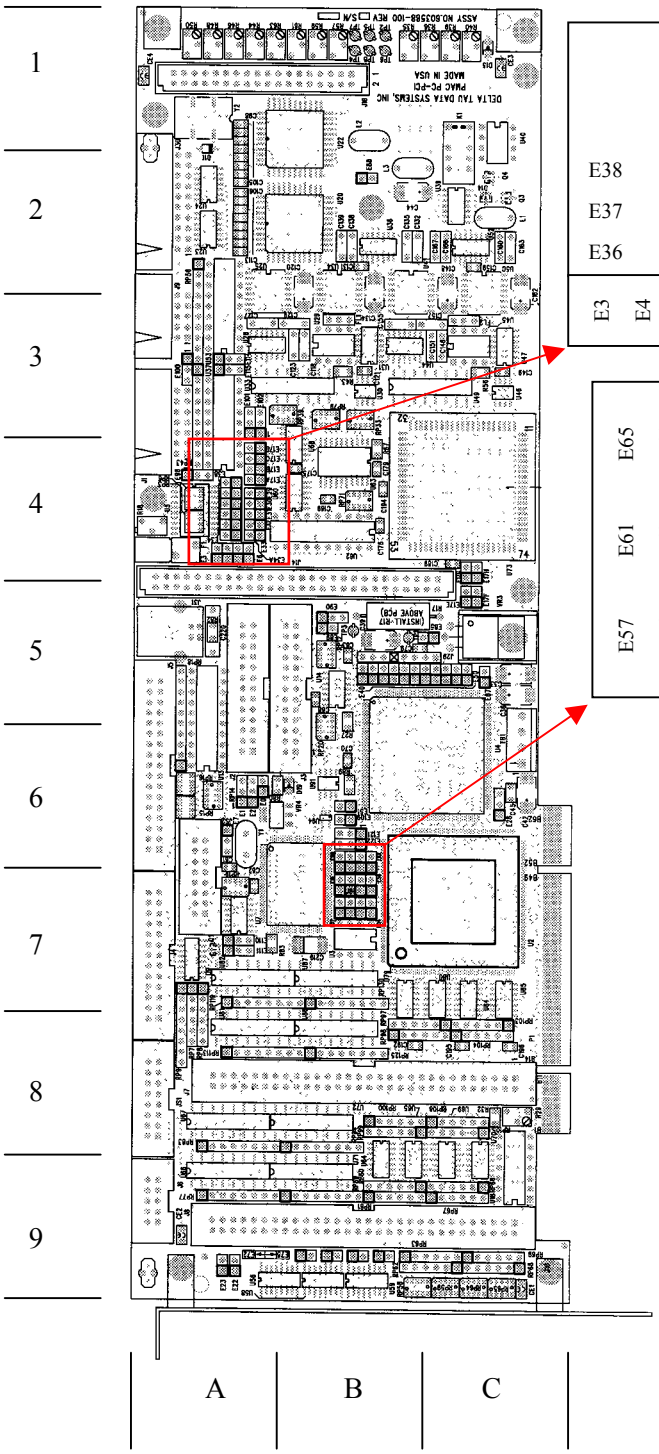
LED Indicators

PMACs with the Option CPU have three LED indicators: red, yellow, and green. The red and green LEDs have the same meaning as with the standard CPU: when the green LED is lit, this indicates that power is applied to the +5V input; when the red LED is lit, this indicates that the watchdog timer has tripped and shut down the PMAC.

The yellow LED located beside the red and green LEDs, when lit, indicates that the phase-locked loop that multiplies the CPU clock frequency from the crystal frequency on the Option CPU is operational and stable. This indicator is for diagnostic purposes only; it may not be present on all boards.

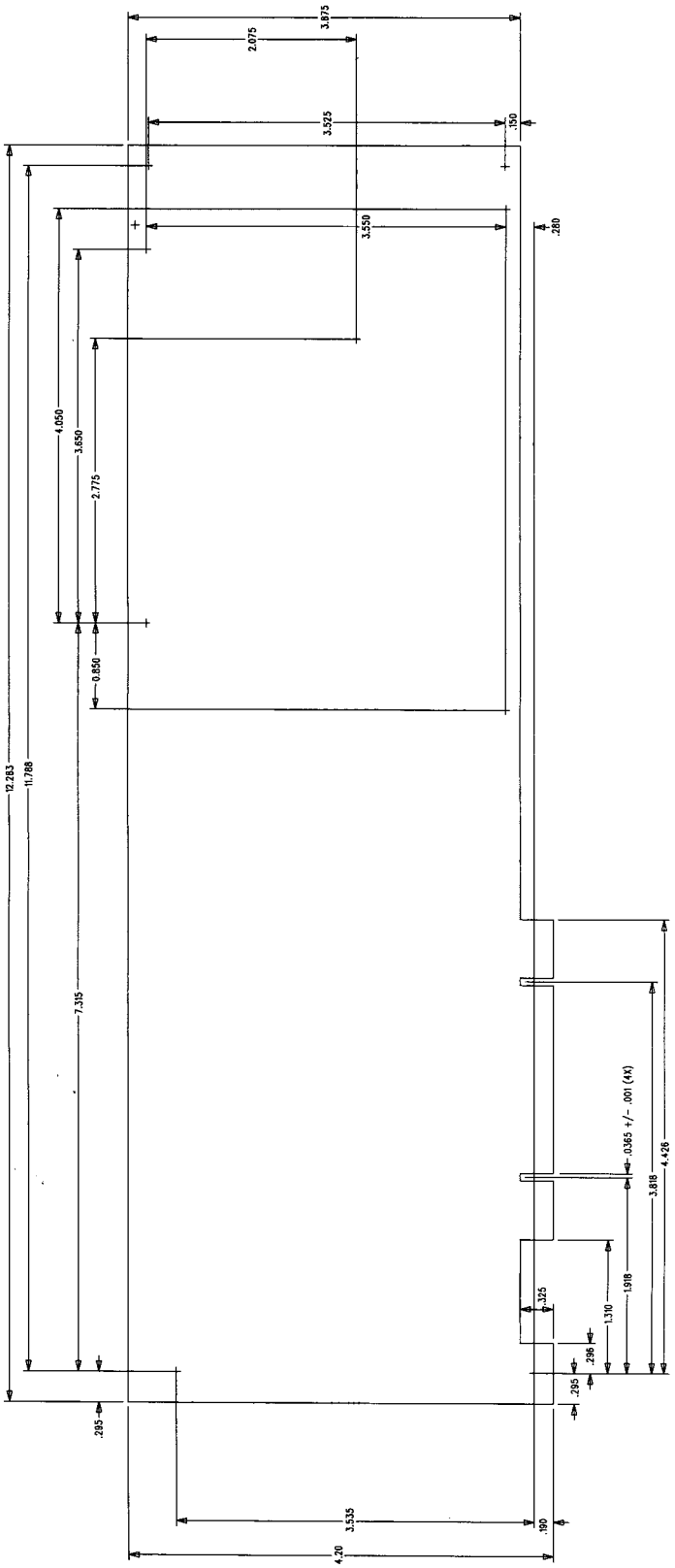
The PMAC PCI has an interlock circuit that drops out the ±15V supplies to the analog outputs through a fail-safe relay if any supply on PMAC is lost. In this case the green LED D15 will be off. The D19 LED will be lit when 5V is applied to PMAC.

PMAC Board Layout Part Number 603588-100



Feature	Location	Feature	Location
E0	A6	E57	B7
E1	A6	E58	B7
E2	A6	E59	B7
E3	A4	E60	B7
E4	A4	E61	B7
E5	A4	E62	B6
E6	A4	E63	B6
E7	A6	E64	B6
E17A	A4	E65	B6
E17B	A4	E72	B9
E17C	A4	E73	B9
E17D	A4	E74	B9
E17E	C5	E75	B9
E17F	C5	E85	C5
E17G	C4	E87	C5
E17H	C4	E88	B2
E22	A9	E89	B5
E23	A9	E90	B5
E28	C6	E98	A4
E29	A4	E100	A3
E30	A4	E101	A3
E31	A4	E102	A3
E32	A4	E109	B6
E33	A4	E110	A7
E34	A4	E111	A7
E34A	A4	E114	A3
E35	A4	E115	A3
E36	A4	E121	B6
E37	A4	E122	B6
E38	A4	D15	C1
E40	B5	D19	B6
E41	B5	J1	A4
E42	B5	J2	A6
E43	B5	J3	B6
E44	B5	J4	A7
E45	B5	J5	A5
E46	C5	J6	A9
E47	C5	J7	A8
E48	C5	J8	A9
E49	C5	J9	A2
E50	C5	J30	A1
E51	B6	J31	A5
E54	B7	JS1	A8
E55	B7	JS2	A6
E56	B7	TB1	C6

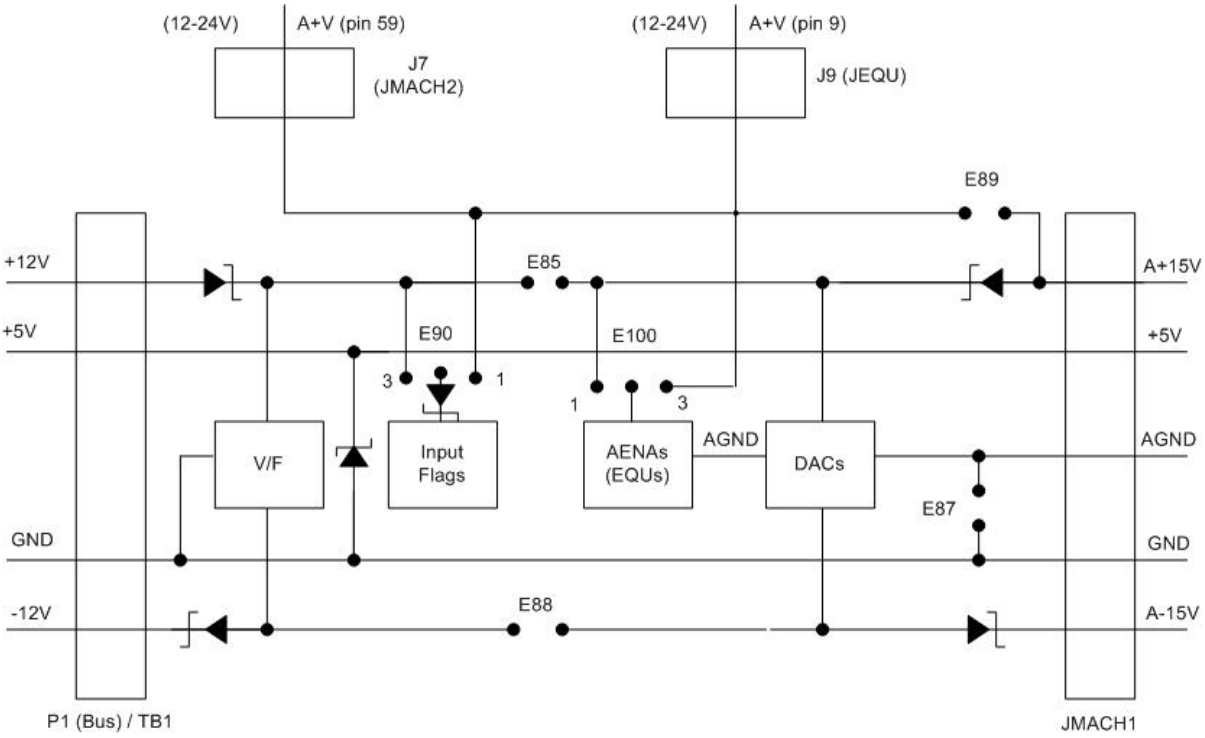
PMAC Board Dimensions Part Number 603588-100



JUMPER SUMMARY

On the PMAC there are many jumpers (pairs of metal prongs), called E-points. Some have been shorted together; others have been left open. These jumpers customize the hardware features of the board for a given application and must be set up appropriately. The following is an overview of the various PMAC jumpers grouped in appropriate categories. For a complete description of the jumper setup configuration please refer to the PMAC PCI CPU Board E-Point Descriptions chapter of this manual.

Power-Supply Configuration Jumpers



E85, E87, E88: Analog Circuit Isolation Control – These jumpers control whether the analog circuitry on the PMAC PCI is isolated from the digital circuitry, or electrically tied to it. In the default configuration, these jumpers are off, keeping the circuits isolated from each other (provided separate isolated supplies are used).

E89-E90: Input Flag Supply Control – If E90 connects pins 1 and 2 and E89 is on, the input flags (+LIMn, -LIMn, and HMFLn) are supplied from the analog A+15V supply, which can be isolated from the digital circuitry. If E90 connects pins 1 and 2 and E89 is off, the input flags are supplied from a separate A+V supply brought in on pin 59 of the J7 JMACH2 connector. This supply can be in the +12V to +24V range, and can be kept isolated from the digital circuitry. If E90 connects pins 2 and 3, the input flags are supplied from the digital +12V supply, and isolation from the digital circuitry is defeated.

E100: AENA/EQU Supply Control – If E100 connects pins 1 and 2, the circuits related to the AENAn, EQUn and FAULTn signals will be supplied from the analog A+15V supply, which can be isolated from the digital circuitry. If E100 connects pins 2 and 3, the circuits will be supplied from a separate A+V supply brought in on pin 9 of the J9 JEQU connector. This supply can be in the +12V to +24V range and can be kept isolated from the digital circuitry.

Clock Configuration Jumpers

E3-E6: Servo Clock Frequency Control – The jumpers E3 – E6 determine the servo-clock frequency by controlling how many times it is divided down from the phase frequency. The default setting of E3 and E4 off, E5 and E6 on divides the phase-clock frequency by 4, creating a 2.25 kHz servo-clock frequency. This setting is seldom changed.

E29-E33: Phase Clock Frequency Control – Only one of the jumpers E29 – E33, which select the phase-clock frequency, may be on in any configuration. The default setting of E31 on, which selects a 9 kHz phase-clock frequency, is seldom changed.

E34-E38: Encoder Sample Clock – Only one of the jumpers E34 – E38, which select the encoder sample clock frequency, may be on in any configuration. The frequency must be high enough to accept the maximum true count rate (no more than one count in any clock period), but a lower frequency can filter out longer noise spikes. The anti-noise digital delay filter can eliminate noise spikes up to one sample-clock cycle wide.

E40-43: Servo and Phase Clock Direction Control – Jumpers E40-E43 control the software address of the card for serial addressing and for sharing the servo and phase clock over the serial connector. Card @0 sends the clocks and cards @1-@F receive the clocks. If any of these jumpers is removed, PMAC PCI will expect to receive external servo and phase clock signals on the J4 serial port. If these signals are not provided in this configuration, the watchdog timer will immediately trip.

E98: DAC/ADC Clock Frequency Control – Leave E98 in its default setting of 1-2, which creates a 2.45 MHz DCLK signal, unless connecting an ACC-28 A/D-converter board. In this case, move the jumper to connect pins 2 and 3, which creates a 1.22 MHz DCLK signal.

Encoder Configuration Jumpers

Encoder Complementary Line Control – The selection of the type of encoder used, either single ended or differential is made through the resistor packs configuration and not through a jumper configuration.

E22-E23: Control-Panel Handwheel Enable – Putting these jumpers on ties the handwheel-encoder inputs on the JPAN control-panel port to the Channel 2 encoder circuitry. If the handwheel inputs are connected to Channel 2, no encoder should be connected to Channel 2 through the JMACH1 connector.

E72-E73: Control Panel Analog Input Enable – Putting these jumpers on ties the output of the Option 10 voltage-to-frequency converter that can process the WIPER analog input on the JPAN control panel port to the Channel 4 encoder circuitry. If the frequency signal is connected to Channel 4, no encoder should be connected to Channel 4 through the JMACH1 connector.

E74-E75: Encoder Sample Clock Output – Putting these jumpers on ties the encoder sample-clock signal to the CHC4 and CHC4/ lines on the JMACH1 port. This permits the clock signal to be used to synchronize external encoder-processing devices like the ACC-8D Option 8 interpolator board. With these jumpers on, no encoder input signal should be connected to these pins.

Board Reset/Save Jumpers

E50: Flash-Save Enable/Disable Control – If E50 is on (default), the active software configuration of the PMAC can be stored to non-volatile flash memory with the **SAVE** command. If the jumper on E50 is removed, this **SAVE** function is disabled, and the contents of the flash memory cannot be changed.

E51: Re-Initialization on Reset Control – If E51 is off (default), PMAC executes a normal reset, loading active memory from the last saved configuration in non-volatile flash memory. If E51 is on, PMAC re-initializes on reset, loading active memory with the factory default values.

Communication Jumpers

PCI Bus Base Address Control – The selection of the base address of the card in the I/O space of the host PC's expansion bus is assigned automatically by the operating system and it is not selected through a jumper configuration.

E49: Serial Communications Parity Control – Jump pin 1 to 2 for no serial parity; remove jumper for ODD serial parity.

E54-E65: Interrupt Source Control – These jumpers control which signals are tied to interrupt lines IR5, IR6 and IR7 on PMAC's programmable interrupt controller (PIC), as shown in the interrupt diagram. Only one signal may be tied into each of these lines.

E110: Serial Port Configure – Jump pin 1 to 2 for use of the J4 connector as RS-232. Jump pin 2 to 3 for use of the J4 connector as RS-422.

E111: Clock Lines Output Enable – Jump pin 1 to 2 to enable the Phase, Servo and Init lines on the J4 connector. Jump pin 2 to 3 to disable the Phase, Servo and Init lines on the J4 connector. E111 on positions one to two is necessary for daisy-chained PMACs sharing the clock lines for synchronization.

I/O Configuration Jumpers

Caution:

A wrong setting of these jumpers will damage the associated output IC.

E1-E2: Machine Output Supply Configure – With the default sinking output driver IC (ULN2803A or equivalent) in U13 for the J5 JOPTO port outputs, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly.

E7: Machine Input Source/Sink Control – With this jumper connecting pins 1 and 2 (default), the machine input lines on the J5 JOPTO port are pulled up to +5V or the externally provided supply voltage for the port. This configuration is suitable for sinking drivers. If the jumper is changed to connect pins 2 and 3, these lines are pulled down to GND. This configuration is suitable for sourcing drivers.

E17A - E17D: Motors 1-4 Amplifier-Enable Polarity Control – Jumpers E17A through E17D control the polarity of the amplifier enable signal for the corresponding motor 1 to 4. When the jumper is on (default), the amplifier-enable line for the corresponding motor is low true so the enable state is low-voltage output and sinking current, and the disable state is not conducting current. With the default ULN2803A sinking driver used by the PMAC PCI on U37, this is the fail-safe option, allowing the circuit to fail in the disable state. With this jumper off, the amplifier-enable line is high true so the enable state is not conducting current, and the disable state is low-voltage output and sinking current. This setting is not generally recommended.

E17E - E17H: Motors 5-8 Amplifier-Enable Polarity Control – Jumpers E17A through E17D control the polarity of the amplifier enable signal for the corresponding motor 5 to 8. When the jumper is on (default), the amplifier-enable line for the corresponding motor is low true so the enable state is low-voltage output and sinking current, and the disable state is not conducting current. With the default ULN2803A sinking driver used by the PMAC PCI on U53, this is the fail-safe option, allowing the circuit to fail in the disable state. With this jumper off, the amplifier-enable line is high true so the enable state is not conducting current and the disable state is low-voltage output and sinking current. This setting is not generally recommended.

E28: Following-Error/Watchdog-Timer Signal Control – With this jumper connecting pins 2 and 3 (default), the FEFCO/ output on pin 57 of the J8 JMACH1 servo connector outputs the watchdog timer signal. With this jumper connecting pins 1 and 2, this pin outputs the warning following error status line for the selected coordinate system.

Caution:

A wrong setting of these jumpers will damage the associated output IC.

E101-E102: Motors 1-4 AENA/EQU Voltage Configure – The U37 driver IC controls the AENA and EQU signals of motors 1 to 4. With the default sinking output driver IC (ULN2803A or equivalent) in U37, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly.

Caution:

A wrong setting of these jumpers will damage the associated output IC.

E114-E115: Motors 5-8 AENA/EQU Voltage Configure – The U53 driver IC controls the AENA and EQU signals of motors 5 to 8. With the default sinking output driver IC (ULN2803A or equivalent) in U53, these jumpers must connect pins 1 and 2 to supply the IC correctly. If this IC is replaced with a sourcing output driver IC (UDN2981A or equivalent), these jumpers must be changed to connect pins 2 and 3 to supply the new IC correctly.

E121: XIN6 Motor Selection – Jump 1-2 to bring the QuadLoss signal for Encoder 6 into register XIN6 at Y:$070801 bit 6. Jump 2-3 to bring the QuadLoss signal for Encoder 7 into register XIN6 at Y:$070801 bit 6.

E122: XIN7 Feature Selection – Jump 1-2 to bring the QuadLoss signal for Encoder 8 into register XIN7 at Y:$070801 bit 7. Jump 2-3 to bring the PowerGood signal into register XIN7 at Y:$070801 bit 7.

Reserved Configuration Jumpers

E109: Reserved for Future Use

Piggyback Turbo CPU Board Jumper Configuration

Watchdog Timer Jumper

Jumper E1 on the Turbo CPU board must be off for the watchdog timer to operate. This is a very important safety feature, so it is vital that this jumper be off in normal operation. E1 should only be put on to debug problems with the watchdog timer circuit.

Dual-Ported RAM Source Jumper

On Turbo CPU boards with revision suffixes – 10A and newer, Jumper E2 must connect pins 1 and 2 to access dual-ported RAM (addresses $06xxxx) from the baseboard. If using the Option 2 DPRAM on the baseboard, jumper E2 must be in this setting.

Jumper E2 must connect pins 2 and 3 to access dual-ported RAM (addresses $06xxxx) through the JEXP expansion port. If using DPRAM on an external accessory board, Jumper E2 must be in this setting.

On Turbo CPU boards with revision suffixes 109 and older, there is no jumper for this purpose, and the boards can access DPRAM from either source, but with less robust buffering.

Power-Up State Jumpers

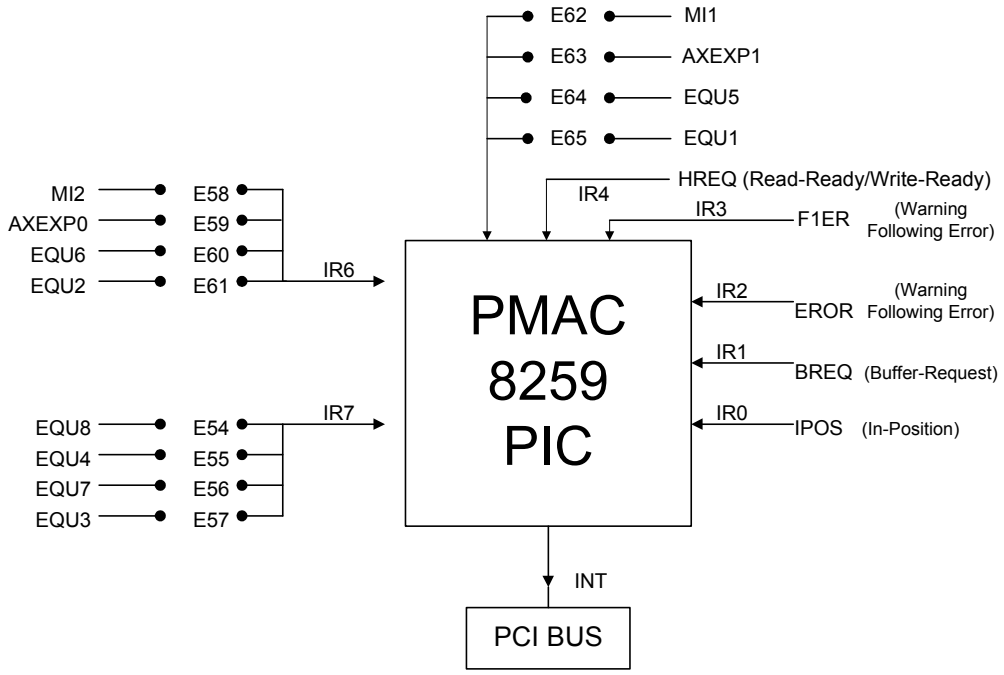
Jumper E4 on the Turbo CPU board must be off, Jumper E5 must be on, and Jumper E6 must be on, in order for the CPU to copy the firmware from flash memory into active RAM on power-up/reset. This is necessary for normal operation of the card. (Other settings are for factory use only.)

Firmware Load Jumper

If Jumper E7 on the CPU board is on during power-up/reset, the board comes up in bootstrap mode, which permits the loading of new firmware into the flash-memory IC on the board. When the PMAC Executive program tries to establish communications with a board in this mode, it will detect that the board is in bootstrap mode automatically and ask what file to download as the new firmware.

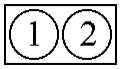
Jumper E7 must be off during power-up/reset for the board to come up in normal operational mode.

PMAC-PC INTERRUPT STRUCTURE



CPU BOARD E-POINT DESCRIPTIONS

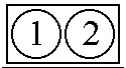
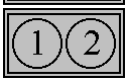
E1: Watchdog Disable Jumper

E Point and Physical Layout	Description	Default
E1 	Jump pin 1 to 2 to disable Watchdog timer (for test purposes only). Remove jumper to enable Watchdog timer.	No jumper installed

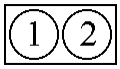
E2: DPRAM Location Configure

E Point and Physical Layout	Description	Default
E2 	Jump pin 1 to 2 to access the dual-ported RAM on baseboard. Jump pin 2 to 3 to access the dual-ported RAM through JEXP expansion port.	Jumper connects pins 1 and 2
Note: Jumper E2 is present on –108 and newer boards only. Older versions could access DPRAM from either source without a jumper configuration, but with less robust buffering.		

E4 – E6: Power-Up/Reset Load Source

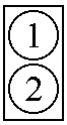
E Point and Physical Layout	Description	Default
E4   **E6**	Remove jumper E4; jump E5 pin 1 to 2; jump E6 pin 1 to 2 to read flash IC on power-up/reset.	No E4 jumper installed; E5 and E6 jump pin 1 to 2.
Note: Other combinations are for factory use only; the board will not operate in any other configuration		

E7: Firmware Reload Enable

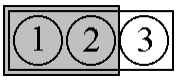
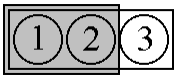
E Point and Physical Layout	Description	Default
E7 	Jump pin 1 to 2 to reload firmware through serial or bus port. Remove jumper for normal operation.	No jumper installed

MAIN BOARD E-POINT DESCRIPTIONS

E0: Machine Output

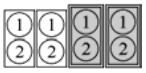
E Point and Physical Layout	Location	Description	Default
E0 	A6	Jump pin 1 to 2 To provide use of 5V outputs	No jumper

E1 - E2: Machine Output Supply Voltage Configure

E Point and Physical Layout	Location	Description	Default
E1 	A6	Jump pin 1 to 2 to apply +V (+5V to 24V) to pin 10 of U13 (should be ULN2803A for sink output configuration) JOPTO Machine outputs M01-M08. ***Caution:*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 2 to 3 to apply GND to pin 10 of U13 (should be UDN2981A for source output configuration).	1-2 Jumper installed
E2 	A6	Jump pin 1 to 2 to apply GND to pin 10 of U13 (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply +V (+5V to 24V) to pin 10 of U13 (should be UDN2981A for source output configuration). ***Caution:*** The jumper setting must match the type of driver IC, or damage to the IC will result.	1-2 Jumper installed

E3 - E6: Servo Clock Frequency Control

The servo clock (which determines how often the servo loop is closed) is derived from the phase clock (see E98, E29 - E33) through a divide-by-N counter. Jumpers E3 through E6 control this dividing function.

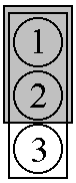
E3	E4	E5	E6	Servo Clock = Phase Clock Divided by N	Default and Physical Layout E3 E4 E5 E6  Location A4 A4 A4 A4
ON	ON	ON	ON	N = Divided by 1	
OFF	ON	ON	ON	N = Divided by 2	
ON	OFF	ON	ON	N = Divided by 3	
OFF	OFF	ON	ON	N = Divided by 4	Only E5 and E6 On
ON	OFF	ON	ON	N = Divided by 5	
OFF	ON	OFF	ON	N = Divided by 6	
ON	OFF	OFF	ON	N = Divided by 7	
OFF	OFF	OFF	ON	N = Divided by 8	
ON	ON	ON	OFF	N = Divided by 9	
OFF	ON	ON	OFF	N = Divided by 10	
ON	OFF	ON	OFF	N = Divided by 11	
OFF	OFF	ON	OFF	N = Divided by 12	
ON	ON	OFF	OFF	N = Divided by 13	
OFF	ON	OFF	OFF	N = Divided by 14	
ON	OFF	OFF	OFF	N = Divided by 15	
OFF	OFF	OFF	OFF	N = Divided by 16	

Note: The setting of I-variable I10 should be adjusted to match the servo interrupt cycle time set by E98, E3 to E6, E29 to E33, and the crystal clock frequency. I10 holds the length of a servo interrupt cycle, scaled so that 8,388,608 equals one millisecond. Since I10 has a maximum value of 8,388,607, the servo interrupt cycle time should always be less than a millisecond (unless you want to make your basic unit of time on PMAC something other than a millisecond). If you wish a servo sample time greater than one millisecond, the sampling may be slowed in software with variable Ix60.

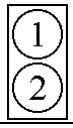
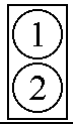
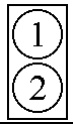
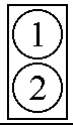
Note: If E40 to E43 are not all on, the phase clock is received from an external source through the J4 serial-port connector, and the settings of E3 – E6 are not relevant.

Frequency can be checked on J4 pins 21 & 22. It can also be checked from the software by typing RX:0 in the PMAC terminal at 10-second intervals and dividing the difference of successive responses by 10000. The resulting number is the approximate Servo Clock frequency kHz.

E7: Machine Input Source/Sink Control

E Point and Physical Layout	Location	Description	Default
E7 	A6	Jump pin 1 to 2 to apply +5V to input reference resistor sip pack; this will bias MI1 to MI8 inputs to +5V for OFF state; input must then be grounded for ON state. Jump pin 2 to 3 to apply GND to input reference resistor sip pack; this will bias MI1 to MI8 inputs to GND for OFF state; input must then be pulled up for ON state (+5V to +24V).	1-2 Jumper installed

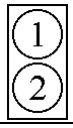
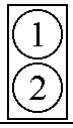
E17A-D: Amplifier Enable/Direction Polarity Control

E Point and Physical Layout	Location	Description	Default
E17A 	A4	Jump 1-2 for high-true AENA1. Remove jumper for low-true AENA1.	No jumper installed
E17B 	A4	Jump 1-2 for high-true AENA2. Remove jumper for low-true AENA2.	No jumper installed
E17C 	A4	Jump 1-2 for high-true AENA3. Remove jumper for low-true AENA3.	No jumper installed
E17D 	A4	Jump 1-2 for high-true AENA4. Remove jumper for low-true AENA4.	No jumper installed
Note: Low-true enable is the fail-safe option because of the sinking (open-collector) ULN2803A output driver IC.			

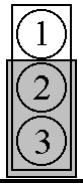
E17E-H: Amplifier Enable/Direction Polarity Control

E Point and Physical Layout	Location	Description	Default
E17E	C5	Jump 1-2 for high-true AENA5. Remove jumper for low-true AENA1.	No jumper installed
E17F	C5	Jump 1-2 for high-true AENA6. Remove jumper for low-true AENA2.	No jumper installed
E17G	C4	Jump 1-2 for high-true AENA7. Remove jumper for low-true AENA3.	No jumper installed
E17H	C4	Jump 1-2 for high-true AENA8. Remove jumper for low-true AENA4.	No jumper installed
Note: Low-true enable is the fail-safe option because of the sinking (open-collector) ULN2803A output driver IC.			

E22 - E23: Control Panel Handwheel Enable

E Point and Physical Layout	Location	Description	Default
E22 	A9	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-16 for CHB2 (ENC2-B).	No jumper
E23 	A9	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-22 for CHA2 (ENC2-A).	No jumper
Note: With these jumpers on, no encoder should be wired into ENC2 on JMACH1. Jumper E26 must connect pins 1-2, because these are single-ended inputs. This function is unrelated to the encoder brought in through ACC-39 on J2.			

E28: Following Error/Watchdog Timer Signal Control

E Point and Physical Layout	Location	Description	Default
E28 	C6	Jump pin 1 to 2 to allow warning following error (Ix12) for the selected coordinate system to control FEFCO/ on J8-57. Jump pin 2 to 3 to cause Watchdog timer output to control FEFCO/. Low true output in either case.	2-3 Jumper installed

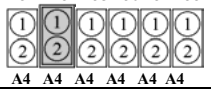
E29 - E33: Phase Clock Frequency Control

Jumpers E29 through E33 control the speed of the phase clock, and, indirectly, the servo clock, which is divided down from the phase clock (see E3 - E6). No more than one of these five jumpers may be on at a time.

					Phase Clock Frequency		Default and Physical Layout	Location
E29	**E30**	**E31**	**E32**	**E33**	**E98 Connects Pins 1 and 2**	**E98 Connects Pins 2 And 3**		
ON	OFF	OFF	OFF	OFF	2.26 kHz	1.13 kHz	**E29**	A4
OFF	ON	OFF	OFF	OFF	4.52 kHz	2.26 kHz	**E30**	A4
OFF	OFF	ON	OFF	OFF	9.04 kHz	4.52 kHz	**E31**	A4
OFF	OFF	OFF	ON	OFF	18.07 kHz	9.04 kHz	**E32**	A4
OFF	OFF	OFF	OFF	ON	36.14 kHz	18.07 kHz	**E33**	A4
Note: If E40 to E43 are not all on, the phase clock is received from an external source through the J4 serial-port connector and the settings of E29 – E33 are not relevant.								

E34 - E38: Encoder Sampling Clock Frequency Control

Jumpers E34 - E38 control the encoder-sampling clock (SCLK) used by the gate array ICs. No more than one of these six jumpers may be on at a time.

						SCLK Clock Frequency	Default and Physical Layout
E34A	**E34**	**E35**	**E36**	**E37**	**E38**		E34A E34 E35 E36 E37 E38  A4 A4 A4 A4 A4 A4
ON	OFF	OFF	OFF	OFF	OFF	19.6608 MHz	
OFF	ON	OFF	ON	OFF	OFF	9.8304 MHz	E34 On
OFF	OFF	ON	OFF	OFF	OFF	4.9152 MHz	
OFF	OFF	OFF	ON	OFF	OFF	2.4576 MHz	
OFF	OFF	OFF	OFF	ON	OFF	1.2288 MHz	
OFF	OFF	OFF	OFF	OFF	ON	External clock 1 to 30 MHz maximum output on CHC4 and CHC4/	

E40 - E43: Software Address Control

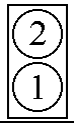
Jumpers E40–E43 control the software address of the card, for serial addressing and for sharing the servo and phase clock over the serial connector. Card @0 sends the clocks and cards @1–@F receive the clocks.

Card Address Control E Points					Default and Physical Layout E40 E41 E42 E43
E40	**E41**	**E42**	**E43**	**Card Address**	LOCATION B5 B5 B5 B5
ON	ON	ON	ON	@0	@0
OFF	ON	ON	ON	@1	
ON	OFF	ON	ON	@2	
OFF	OFF	ON	ON	@3	
ON	ON	OFF	ON	@4	
OFF	ON	OFF	ON	@5	
ON	OFF	OFF	ON	@6	
OFF	OFF	OFF	ON	@7	
ON	ON	ON	OFF	@8	
OFF	ON	ON	OFF	@9	
ON	OFF	ON	OFF	@A	
OFF	OFF	ON	OFF	@B	
ON	ON	OFF	OFF	@C	
OFF	ON	OFF	OFF	@D	
ON	OFF	OFF	OFF	@E	
OFF	OFF	OFF	OFF	@F	

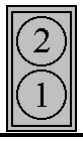
Note: The card must be set up either as @0, or receiving clock signals over the serial port from another card that is set up as @0, or the Watchdog timer will trip (red light on) and the card will shut down.

E48: CPU Clock Frequency Control (Option CPU Section)

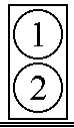
E48 controls the CPU clock frequency only on PMAC with an option CPU section using flash memory backup (no battery). This CPU section is used on PMACs ordered with Opt 4A, 5A, or 5B. The 80 MHz setting of a CPU section ordered with Opt 5C is performed by software; refer to the Software Configuration section of this manual.

E Point and Physical Layout	Location	Description	Default
E48 	C5	Jump pins 1 and 2 to multiply crystal frequency by three inside CPU for 60-MHz operation. Remove jumper to multiply crystal frequency by two inside CPU for 40 MHz operation.	Jumper installed (Option 5, 5B) Jumper not installed (Standard, Option 4A, 5A)
Note: It may be possible to operate a board with 40 MHz components (Option 5A) at 60 MHz under some conditions by changing the setting of jumper E48. However, this operates the components outside of their specified operating range, and proper execution of PMAC under these conditions is not guaranteed. PMAC software failure is possible, even probable, under these conditions, and this can lead to very dangerous machine failure. Operation in this mode is done completely at the user's own risk; Delta Tau cannot accept responsibility for the operation of PMAC or the machine under these conditions.			

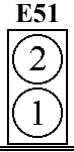
E49: Serial Communications Parity Control

E Point and Physical Layout	Location	Description	Default
E49 	C5	Jump pin 1 to 2 for no serial parity. Remove jumper for odd serial parity.	Jumper installed

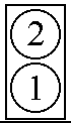
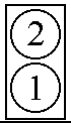
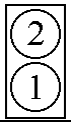
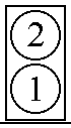
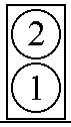
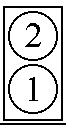
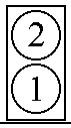
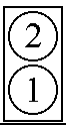
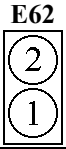
E50: Flash Save Enable/Disable

E Point and Physical Layout	Location	Description	Default
E50 	C5	Jump pin 1 to 2 to enable save to flash memory. Remove jumper to disable save to flash memory.	Jumper Installed

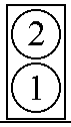
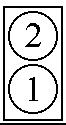
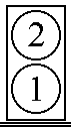
E51: Normal/Re-Initializing Power-Up

E Point and Physical Layout	Location	Description	Default
E51 	B6	Jump pin 1 to 2 to re-initialize On power-up/reset; Remove jumper for Normal power-up/reset.	No jumper installed

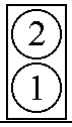
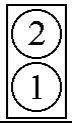
E54 - E65: Host Interrupt Signal Select

E Point and Physical Layout	Location	Description	Default
E54 	B7	Jump pin 1 to 2 to allow EQU8 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E55 	B7	Jump pin 1 to 2 to allow EQU4 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E56 	B7	Jump pin 1 to 2 to allow EQU7 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E57 	B7	Jump pin 1 to 2 to allow EQU3 to interrupt host-PC at PMAC interrupt level IR7.	No jumper installed
E58 	B7	Jump pin 1 to 2 to allow MI2 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E59 	B7	Jump pin 1 to 2 to allow Axis Expansion Int-0 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E60 	B7	Jump pin 1 to 2 to allow EQU6 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E61 	B7	Jump pin 1 to 2 to allow EQU2 to interrupt host-PC at PMAC interrupt level IR6.	No jumper installed
E62 	B6	Jump pin 1 to 2 to allow MI1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed

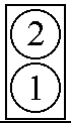
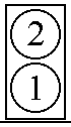
E54-E65 (Continued)

E Point and Physical Layout	Location	Description	Default
E63 	B6	Jump pin 1 to 2 to allow Axis Expansion Int-1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed
E64 	B6	Jump pin 1 to 2 to allow EQU5 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed
E65 	B6	Jump pin 1 to 2 to allow EQU1 to interrupt host-PC at PMAC interrupt level IR5.	No jumper installed

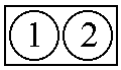
E72 - E73: Panel Analog Time Base Signal Enable

E Point and Physical Layout	Location	Description	Default
E72 	B9	Jump pin 1 to 2 to allow V to F converter FOUT derived from Wiper input on J2 to connect to CHA4.	No jumper installed
E73 	B9	Jump pin 1 to 2 to allow V to F converter FOUT/ derived from Wiper input on J2 to connect to CHA4/.	No jumper installed
Note: With these jumpers On, no encoder should be wired into ENC4 on JMACH1. E27 must connect pins 1 to 2 because these are single-ended inputs. Variable I915 should be set to 4 to create a positive voltage (frequency) number in PMAC.			

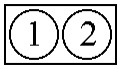
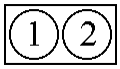
E74 - E75: Clock Output Control for Ext. Interpolation

E Point and Physical Layout	Location	Description	Default
E74 	B9	Jump pin 1 to 2 to allow SCLK/ to output on CHC4/.	No jumper installed
E75 	B9	Jump pin 1 to 2 to allow SCLK to output on CHC4.	No jumper installed
Note: SCLK out permits synchronous latching of analog encoder interpolators such as ACC-8D Opt 8.			

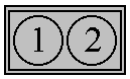
E85: Host-Supplied Analog Power Source Enable

E Point and Physical Layout	Location	Description	Default
E85 	C5	Jump pin 1 to pin 2 to allow A+14V to come from PC bus (ties amplifier and PMAC PCI power supply together. Defeats OPTO coupling.) Also see E90.	No jumper
Note: If E85 is changed, E88 and E87 must also be changed.			

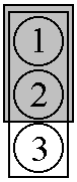
E87 - E88: Host-Supplied Analog Power Source Enable

E Point and Physical Layout	Location	Description	Default
E87 	C5	Jump pin 1 to pin 2 to allow AGND to come from PC bus (ties amplifier and PMAC PCI GND together. Defeats OPTO coupling.) Also see E90.	No jumper
Note: If E87 is changed, E85 and E88 must also be changed.			
E88 	B2	Jump pin 1 to pin 2 to allow A-14V to come from PC bus (ties amplifier and PMAC PCI power supply together. Defeats OPTO coupling.) Also see E90.	No jumper
Note: If E88 is changed; E87 and E85 must also be changed.			

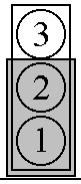
E89: Amplifier-Supplied Switch Pull-Up Enable

E Point and Physical Layout	Location	Description	Default
E89 	B5	Jump pin 1 to 2 to use A+15V on J8 (JMACH1) pin 59 as supply for input flags. Remove jumper to use A+15V/OPT+V from J7 pin 59 as supply for input flags.	Jumper installed
Note: This jumper setting is only relevant if E90 connects pin 1 to 2.			

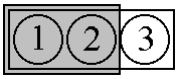
E90: Host-Supplied Switch Pull-Up Enable

E Point and Physical Layout	Location	Description	Default
E90 	B5	Jump pin 1 to 2 to use A+15V from J8 pin 59 as supply for input flags (E89 ON) {flags should be tied to AGND} or A+15V/OPT+V from J7 pin 59 as supply for input flags (E89 OFF) {flags should be tied to separate 0V reference}. Jump pin 2 to 3 to use +12V from PC bus connector P1-pin B09 as supply for input flags {flags should be tied to GND}.	1-2 Jumper installed
See also E85, E87, E88 and PMAC Opto-isolation diagram			

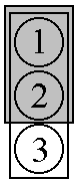
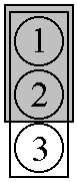
E98: DAC/ADC Clock Frequency Control

E Point and Physical Layout	Location	Description	Default
E98 	A4	Jump 1-2 to provide a 2.45 MHz DCLK signal to DACs and ADCs. Jump 2-3 to provide a 1.22 MHz DCLK signal to DACs and ADCs. Important for high accuracy A/D conversion on ACC-28.	1-2 Jumper installed
Note: This also divides the phase and servo clock frequencies in half. See E29-E33, E3-E6, I10			

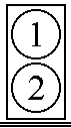
E100: Output Flag Supply Select

E Point and Physical Layout	Location	Description	Default
E100 	A3	Jump pin 1 to 2 to apply analog supply voltage A+15V to U37 and U53 flag output driver IC. Jump pin 2 to 3 to apply flag supply voltage OPT+V to U37 and U53 flag output driver IC.	1-2 Jumper installed

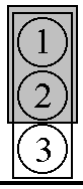
E101 - E102: Motors 1-4 Amplifier Enable Output Configure

E Point and Physical Layout	Location	Description	Default
E101 	A3	***Caution:*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply A+15V/A+V (as set by E100) to pin 10 of U37 AENAn and EQUn driver IC (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply GND to pin 10 of U37 (should be UDN2981A for source output configuration).	1-2 Jumper installed
E102 	A3	***Caution:*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply GND to pin 10 of U37 AENAn and EQUn (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply A+15V/A+V (as set by E100) to pin 10 of U37 (should be UDN2981A for source output configuration).	1-2 Jumper installed

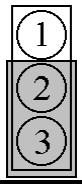
E109: Reserved for Future Use

E Point and Physical Layout	Location	Description	Default
E109 	B6	For future use.	No jumper

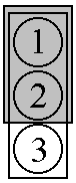
E110: Serial Port Configure

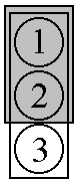
E Point and Physical Layout	Location	Description	Default
E110 	A7	Jump pin 1 to 2 for use of the J4 connector as RS-232. Jump pin 2 to 3 for use of the J4 connector as RS-422.	1-2 Jumper installed

E111: Clock Lines Output Enable

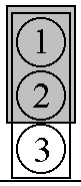
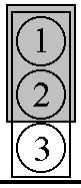
E Point and Physical Layout	Location	Description	Default
E111 	A7	Jump pin 1 to 2 to enable the Phase, Servo and Init lines on the J4 connector. Jump pin 2 to 3 to disable the Phase, Servo and Init lines on the J4 connector. E111 on positions 1 to 2 is necessary for daisy-chained PMACs sharing the clock lines for synchronization.	2-3 Jumper installed

E114 - E115: Motors 5-8 Amplifier Enable Output Configure

E Point and Physical Layout	Location	Description	Default
E114 	A3	***Caution:*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply A+15V/A+V (as set by E100) to pin 10 of U53 AENAn and EQUn driver IC (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply GND to pin 10 of U53 (should be UDN2981A for source output configuration).	1-2 Jumper installed

E115  	A3	***Caution:*** **The jumper setting must match the type of driver IC, or damage to the IC will result.** Jump pin 1 to 2 to apply GND to pin 10 of U53 AENAn and EQUn (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply A+15V/A+V (as set by E100) to pin 10 of U53 (should be UDN2981A for source output configuration).	1-2 Jumper installed

E121 - E122: XIN Feature Selection

E Point and Physical Layout	Location	Description	Default
E121  	F1	Jump 1-2 to bring the QuadLoss signal for Encoder 7 into register XIN6 at Y:$070801 bit 6. Jump 2-3 to bring the QuadLoss signal for Encoder 6 into register XIN6 at Y:$070801 bit 6.	1-2 Jumper installed
E122  	F1	Jump 1-2 to bring the PowerGood signal into register XIN7 at Y:$070801 bit 7. Jump 2-3 to bring the QuadLoss signal for Encoder 8 into register XIN7 at Y:$070801 bit 7.	1-2 Jumper installed

MACHINE CONNECTIONS

Typically, the user connections are made to a terminal block that is attached to the JMACH connector by a flat cable (Acc-8D or 8P). The pinout numbers on the terminal block are the same as those on the JMACH connector. The possible choices for breakout boards are the following:

Board	Mounting	Breakout Style	Breakout Connector	Notes
Acc-8P	DIN – Rail	Monolithic	Terminal Block	Simple Phoenix contact board
Acc-8D	DIN – Rail	Monolithic	Terminal Block	Headers for connection to option boards
Acc-8DCE	DIN – Rail	Modular	D-sub connector	Fully shielded for easy CE mark compliance
Acc-8DP	Panel	Modular	D-sub connector	Used in the PC-pack product

Mounting

The PMAC PCI can be mounted in one of two ways: in the PCI bus, or using standoffs.

- PCI bus: To mount in the PCI bus, simply insert the P1 card-edge connector into PCI socket. If there is a standard PC-style housing, a bracket at the end of the PMAC PCI board can be used to screw into the housing to hold the board down firmly.
- Standoffs: At each of the 4 corners of the PMAC PCI board, there are mounting holes that can be used to mount the board on standoffs.

Power Supplies

Digital Power Supply

2A @ +5V (+/-5%) (10 W)
(Eight-channel configuration, with a typical load of encoders)

- If the PMAC is installed in the internal bus, the host computer provides the 5 Volts power supply.
- With the board plugged into the bus, it will pull +5V power from the bus and it cannot be disconnected. In this case, there must be no external +5V supply, or the two supplies will "fight" each other, possibly causing damage. This voltage can be measured between pins 1 and 3 of the terminal block.
- In a stand-alone configuration, when PMAC is not plugged in a computer bus, it will need an external five-volt supply to power its digital circuits. The +5V line from the supply should be connected to pin 1 or 2 of the JMACH connector (usually through the terminal block), and the digital ground to pin 3 or 4. ACC-1x provides different options for the 5 Volts power supply.

Analog Power Supply

0.3A @ +12 to +15V (4.5W)
0.25A @ -12 to -15V (3.8W)
(Eight-channel configuration)

The analog output circuitry on PMAC is optically isolated from the digital computation circuitry, and so requires a separate power supply. This is brought in on the JMACH connector. The positive supply – +12 to +15V – should be brought in on the A+15V line on pin 59. The negative supply – -12 to -15V – should be brought in on the A-15V line on pin 60. The analog common should be brought in on the AGND line on pin 58.

Typically, this supply can come from the servo amplifier; many commercial amplifiers provide such a supply. If this is not the case, an external supply may be used. ACC-2x provides different options for the ± 15V power supply. Even with an external supply, the AGND line should be tied to the amplifier common. It is possible to get the power for the analog circuits from the bus, but doing so defeats optical isolation. In this case, no new connections need to be made. However, be sure that jumpers E85, E87, E88, E89, and E90 are set up for this circumstance. (The card is not shipped from the factory in this configuration.)

Flags Power Supply (Optional)

Each channel of PMAC has four dedicated digital inputs on the machine connector: +LIMn, -LIMn (overtravel limits), HMFLn (home flag), and FAULTn (amplifier fault). If the PMAC is ordered with the Option-1 (8-axis PMAC) these inputs can be kept isolated from other circuits. A power supply from 12 to 24V connected on pin 59 of J7 could be used to power the corresponding opto-isolators. In this case, jumper E89 must be removed and jumper E90 must connect pins 1-2.

Overtravel Limits and Home Switches

When assigned for the dedicated uses, these signals provide important safety and accuracy functions. +LIMn and -LIMn are direction-sensitive overtravel limits that must be actively held low (sourcing current from the pins to ground) to permit motion in their direction. The direction sense of +LIMn and -LIMn is as follows: +LIMn should be placed at the negative end of travel, and -LIMn should be placed at the positive end of travel.

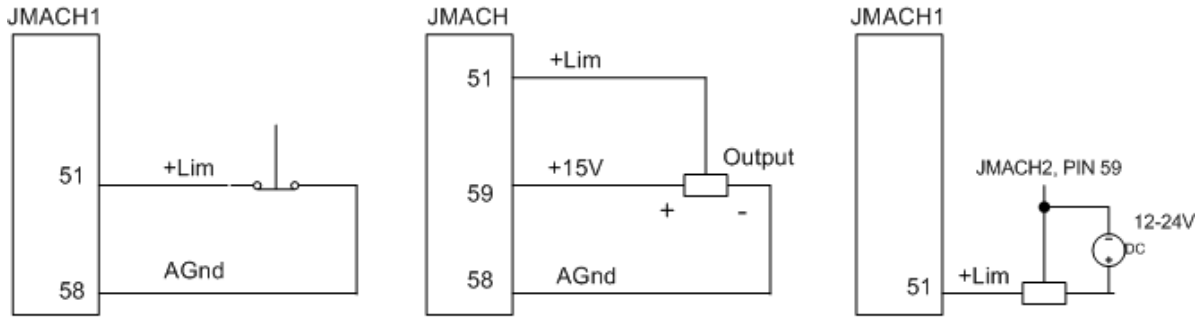
Resistor Pack Configuration: Flag and Digital Inputs Voltage Selection

The PMAC PCI is provided with 6-pin sockets for SIP resistor packs for the input flag sets. Each PMAC PCI is shipped with no resistor packs installed. If the flag or digital inputs circuits are in the 12V to 24V range, no resistor pack should be installed in these sockets. For flags or digital inputs at 5V levels, quad 1kΩ SIP resistor packs (1KSIP6C) should be installed in these sockets. The following table lists the voltage selection resistor pack sockets for each input device:

Device	Resistor Pack	Device	Resistor Pack
Flags 1	RP77	Flags 5	RP113
Flags 2	RP83	Flags 6	RP119
Flags 3	RP89	Flags 7	RP125
Flags 4	RP94	Flags 8	RP130

Types of Overtravel Limits

PMAC expects a closed-to-ground connection for the limits to not be considered on fault. This arrangement provides a failsafe condition and therefore it cannot be reconfigured differently in PMAC. Usually a passive normally closed switch is used. If a proximity switch is needed instead, use a 15V normally closed to ground NPN sinking type sensor.



Dry Contact **15 Volts proximity** **15-24 Volts proximity**

Jumper E89, E90 and E100 must be set appropriately for the type of sensor used.

Home Switches

While normally closed-to-ground switches are required for the overtravel limits inputs, the home switches could be either normally closed or normally open types. The polarity is determined by the home sequence setup, through the I-variables I902, I907, ... I977. However, for the following reasons, the same type of switches used for overtravel limits are recommended:

- Normally closed switches are proven to have greater electrical noise rejection than normally open types.
- Using the same type of switches for every input flag simplifies maintenance stock and replacements.

Motor Signals Connections (JMACH Connectors)

Resistor Pack Configuration: Termination Resistors

The PMAC PCI provides sockets for termination resistors on differential input pairs coming into the board. As shipped, there are no resistor packs in these sockets. If these signals are brought long distances into the PMAC PCI board and ringing at signal transitions is a problem, SIP resistor packs may be mounted in these sockets to reduce or eliminate the ringing.

All termination resistor packs are the type that have independent resistors (no common connection) with each resistor using two adjacent pins. The following table shows which packs are used to terminate each input device:

Device	Resistor Pack	Pack Size	Device	Resistor Pack	Pack Size
Encoder 1	RP61	6-pin	Encoder 5	RP98	6-pin
Encoder 2	RP63	6-pin	Encoder 6	RP100	6-pin
Encoder 3	RP67	6-pin	Encoder 7	RP104	6-pin
Encoder 4	RP69	6-pin	Encoder 8	RP106	6-pin

Resistor Pack Configuration: Differential or Single-Ended Encoder Selection

The differential input signal pairs to the PMAC PCI have user-configurable pull-up/pull-down resistor networks to permit the acceptance of either single-ended or differential signals in one setting, or the detection of lost differential signals in another setting.

The '+' inputs of each differential pair each have a hard-wired 1 kΩ pull-up resistor to +5V. This cannot be changed.

The '-' inputs of each differential pair each have a hard-wired 2.2 kΩ resistor to +5V; each also has another 2.2 kΩ resistor as part of a socketed resistor pack that can be configured as a pull-up resistor to +5V, or a pull-down resistor to GND.

If this socketed resistor is configured as a pull-down resistor (the default configuration), the combination of pull-up and pull-down resistors on this line acts as a voltage divider, holding the line at +2.5V in the absence of an external signal. This configuration is required for single-ended inputs using the '+' lines alone; it is desirable for unconnected inputs to prevent the pick-up of spurious noise; it is permissible for differential line-driver inputs.

If this socketed resistor is configured as a pull-up resistor (by reversing the SIP pack in the socket), the two parallel 2.2 kΩ resistors act as a single 1.1 kΩ pull-up resistor, holding the line at +5V in the absence of an external signal. This configuration is required if encoder-loss detection is desired; it is required if complementary open-collector drivers are used; it is permissible for differential line-driver inputs even without encoder loss detection.

If Pin 1 of the resistor pack (marked by a dot on the pack) matches Pin 1 of the socket (marked by a wide white line on the front side of the board) and a square solder pin on the backside of the board, then the pack is configured as a bank of pull-down resistors. If the pack is reversed in the socket, it is configured as a bank of pull-up resistors.

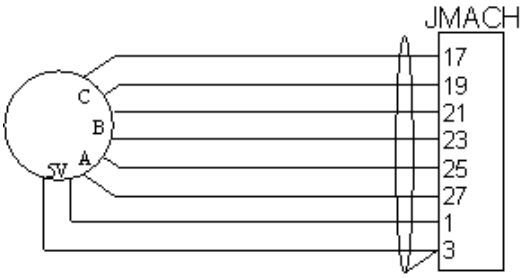
The following table lists the pull-up/pull-down resistor pack for each input device:

Device	Resistor Pack	Pack Size	Device	Resistor Pack	Pack Size
Encoder 1	RP60	6-pin	Encoder 5	RP97	6-pin
Encoder 2	RP62	6-pin	Encoder 6	RP99	6-pin
Encoder 3	RP66	6-pin	Encoder 7	RP103	6-pin
Encoder 4	RP68	6-pin	Encoder 8	RP105	6-pin

Incremental Encoder Connection

Each JMACH connector provides two +5V outputs and two logic grounds for powering encoders and other devices. The +5V outputs are on pins 1 and 2; the grounds are on pins 3 and 4. The encoder signal pins are grouped by number. All those numbered 1 (CHA1, CHA1/, CHB1, CHC1, etc.) belong to encoder #1. The encoder number does not have to match the motor number, but usually does. If the PMAC is not plugged into a bus and drawing its +5V and GND from the bus, use these pins to bring in +5V and GND from the power supply. Connect the A and B (quadrature) encoder channels to the appropriate terminal block pins. For encoder 1, the CHA1 is pin 25, CHB1 is pin 21. If it is a single-ended signal, leave the complementary signal pins floating -- do not ground them. However, if single-ended encoders are used, please check the settings of the jumpers E18 to E21 and E24 to E27. For a differential encoder, connect the complementary signal lines -- CHA1/ is pin 27, and CHB1/ is pin 23. The third channel (index pulse) is optional; for encoder 1, CHC1 is pin 17, and CHC1/ is pin 19.

Example: differential quadrature encoder connected to channel #1:



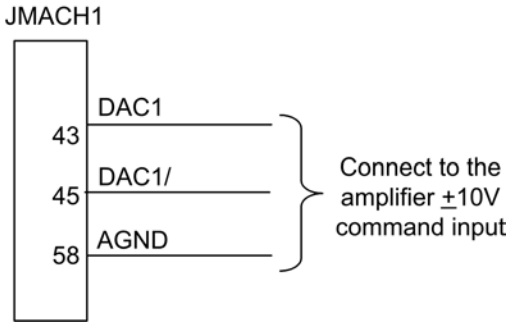
DAC Output Signals

If PMAC is not performing the commutation for the motor, only one analog output channel is required to command the motor. This output channel can be either single-ended or differential, depending on what the amplifier is expecting. For a single-ended command using PMAC channel 1, connect DAC1 (pin 43) to the command input on the amplifier. Connect the amplifier's command signal return line to PMAC's AGND line (pin 58). In this setup, leave the DAC1/ pin floating; do not ground it.

For a differential command using PMAC channel 1, connect DAC1 (pin 43) to the plus command input on the amplifier. Connect DAC1/ (pin 45) to the minus-command input on the amplifier. PMAC's AGND should still be connected to the amplifier common. If the amplifier is expecting separate sign and magnitude signals, connect DAC1 (pin 43) to the magnitude input. Connect AENA1/DIR1 (pin 47) to the sign (direction input). Amplifier signal returns should be connected to AGND (pin 58). This format requires some parameter changes on PMAC; (*see* Ix25. Jumper E17 controls the polarity of the direction output; this may have to be changed during the polarity test. This magnitude-and-direction mode is suited for driving servo amplifiers that expect this type of input, and for driving voltage-to-frequency (V/F) converters, such as PMAC's Acc-8D Option 2 board, for running stepper motor drivers.

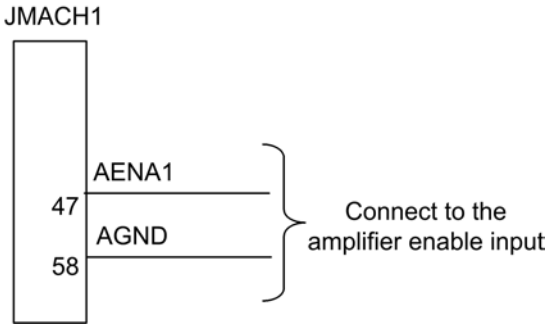
If using PMAC to commutate the motor, use two analog output channels for the motor. Each output may be single-ended or differential, just as for the DC motor. The two channels must be consecutively numbered, with the lower-numbered channel having an odd number (e.g., use DAC1 and DAC2 for a motor, or DAC3 and DAC4, but not DAC2 and DAC3, or DAC2 and DAC4). For our motor #1 example, connect DAC1 (pin 43) and DAC2 (pin 45) to the analog inputs of the amplifier. If using the complements as well, connect DAC1/ (pin 45) and DAC2/ (pin 46) to the minus-command inputs; otherwise leave the complementary signal outputs floating. To limit the range of each signal to +/- 5V, use parameter Ix69. Any analog output not used for dedicated servo purposes may be utilized as a general-purpose analog output. Usually, this is done by defining an M-variable to the digital-to-analog-converter register (suggested M-variable definitions M102, M202, etc.), then writing values to the M-variable. The analog outputs are intended to drive high-impedance inputs with no significant current draw. The 220Ω output resistors will keep the current draw lower than 50 mA in all cases and prevent damage to the output circuitry, but any current draw above 10 mA can result in noticeable signal distortion.

Example:



Amplifier Enable Signal (AENAx/DIRn)

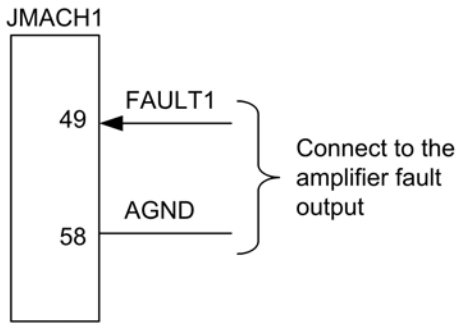
Most amplifiers have an enable/disable input that permits complete shutdown of the amplifier regardless of the voltage of the command signal. PMAC's AENA line is meant for this purpose. If not using a direction and magnitude amplifier or voltage-to-frequency converter, use this pin to enable and disable the amplifier (wired to the enable line). AENA1/DIR1 is pin 47. This signal is an open-collector output with a 3.3 kΩ pull-up resistor to +V, which is a voltage selected by jumper E100. The pull-up resistor packs are RP43 for channels 1-4 and RP-56 for motors 5-8. For early tests, this amplifier signal should be under manual control.



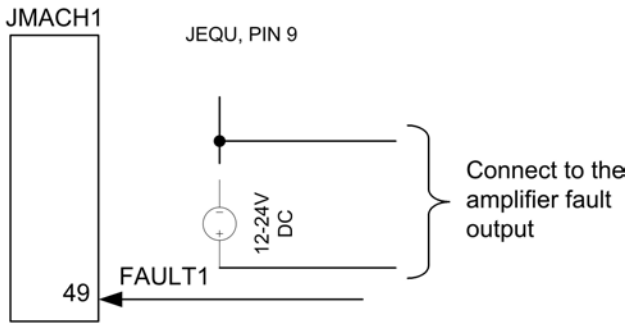
This signal could be either sinking or sourcing as determined by chips U37 and U53 (see jumpers E100-E102 and E114-E115). For 24V, operation E100 must connect pins 2-3 and a separate power supply must be brought on pins 9-7 of the J9 JEQU connector. The polarity of the signal is controlled by jumpers E17A to E17H. The default is low-true (conducting) enable. The amplifier enable signal could also be manually controlled setting Ix00=0 and using the suggested definition of the Mx14 variable.

Amplifier Fault Signal (FAULTn)

This input can take a signal from the amplifier so PMAC knows when the amplifier is having problems, and can shut down action. The polarity is programmable with I-variable Ix25 (I125 for motor #1) and the return signal is analog ground (AGND). FAULT1 is pin 49. With the default setup, this signal must actively be pulled low for a fault condition. In this setup, if nothing is wired into this input, PMAC will consider the motor not to be in a fault condition. The amplifier fault signal can be monitored using the properly defined Mx23 variable.



12-15V signal (E100 on 102)



15-24 Volts Signal (E100 on 2-3)

Some amplifiers share the amplifier fault output with the amplifier enable\disable status output. In this case a special PLC code must be written with the following sequence: disable the amplifier fault input (see Ix25), enable the motor (J/ command), wait for the amplifier fault input to be false (monitor Mx23), re-enable the amplifier fault input (see Ix25).

General-Purpose Digital Inputs and Outputs (JOPTO Port)

PMAC's J5 or JOPTO connector provides eight general-purpose digital inputs and eight general-purpose digital outputs. Each input and each output has its own corresponding ground pin in the opposite row. The 34-pin connector was designed for easy interface to OPTO-22 or equivalent optically isolated I/O modules. Acc-21F is a six-foot cable for this purpose. Characteristics of the JOPTO port on the PMAC PCI:

- 16 I/O points. 100 mA per channel, up to 24V
- Hardware selectable between sinking and sourcing in groups of eight; default is all sinking (inputs can be changed simply by moving a jumper; sourcing outputs must be special-ordered or field-configured)
- Eight inputs, eight outputs only; no changes. Parallel (fast) communications to PMAC CPU
- Not opto-isolated; easily connected to Opto-22 (PB16) or similar modules through ACC-21F cable

Jumper E7 controls the configuration of the eight inputs. If it connects pins 1 and 2 (the default setting), the inputs are biased to +5V for the OFF state and they must be pulled low for the ON state. If E7 connects pins 2 and 3, the inputs are biased to ground for the OFF state, and must be pulled high for the ON state. In either case, a high voltage is interpreted as a 0 by the PMAC software, and a low voltage is interpreted as a 1.

Caution:

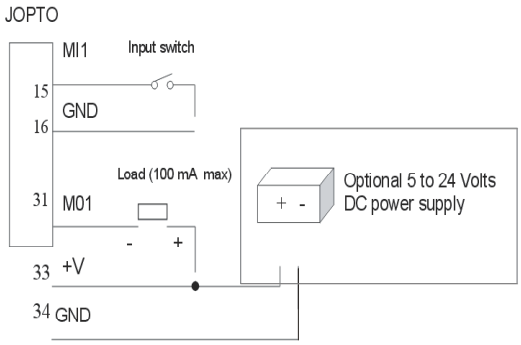
Having Jumpers E1 and E2 set wrong can damage the IC. The +V output on this connector has a 2A fuse, F1, for excessive current protection.

PMAC is shipped standard with a ULN2803A sinking (open-collector) output IC for the eight outputs. These outputs can sink up to 100 mA and have an internal 3.3 kΩ pull-up resistor to go high (RP18). Do not connect these outputs directly to the supply voltage, or damage to the PMAC will result from excessive current draw. A high-side voltage (+5 to +24V) can be provided into Pin 33 of the JOPTO connector, and this can be allowed to pull up the outputs by connecting pins 1 and 2 of Jumper E1. Jumper E2 must also connect pins 1 and 2 for a ULN2803A sinking output.

It is possible for these outputs to be sourcing drivers by substituting a UDN2981A IC for the ULN2803A. This U13 IC is socketed, and so may be replaced easily. For this driver, the internal resistor packs pull down instead. With a UDN2981A driver IC, Jumper E1 must connect pins 2 and 3, and Jumper E2 must connect pins 2 and 3.

The outputs can be configured individually to a different output voltage by removing the internal pull-up resistor pack RP18 and connecting to each output a separate external pull-up resistor to the desired voltage level.

Example: Standard configuration using the ULN2803A sinking (open-collector) output IC



Control-Panel Port I/O (JPAN Port)

The J2 (JPAN) connector is a 26-pin connector with dedicated control inputs, dedicated indicator outputs, a quadrature encoder input, and an analog input. The control inputs are low true with internal pull-up resistors. They have predefined functions unless the control-panel-disable I-variable (I2) has been set to 1. If this is the case, they may be used as general-purpose inputs by assigning M-variable to their corresponding memory-map locations (bits of Y address $78800).

Command Inputs

JOG-/, JOG+/, PREJ/ (return to pre-jog position), and HOME/ affect the motor selected by the FDPn/ lines (see below). The ones that affect a coordinate system are STRT/ (run), STEP/, STOP/ (abort), and HOLD/ (feed hold) affect the coordinate system selected by the FDPn/ lines.

Selector Inputs

The four low-true BCD-coded input lines FDP0/ (LSBit), FDP1/, FDP2/, and FDP3/ (MSBit) form a low-true BCD-coded nibble that selects the active motor and coordinate system (simultaneously). Usually, these are controlled from a single 4-bit motor/coordinate-system selector switch. The motor selected with these input lines will respond to the motor-specific inputs. It will also have its position following function turned on (Ix06 is set to 1 automatically); the motor just de-selected has its position following function turned off (Ix06 is set to 0 automatically).

It is not a good idea to change the selector inputs while holding one of the jog inputs low. Releasing the jog input then will not stop the previously selected motor. This can lead to a dangerous situation.

Alternate Use

The discrete inputs can be used for parallel-data servo feedback or master position if I2 has been set to 1. The Acc-39 Handwheel Encoder Interface board provides 8-bit parallel counter data from a quadrature encoder to these inputs. Refer to the Parallel Position Feedback Conversion section in the Acc-39 User manual for more details on processing this data.

Reset Input

Input INIT/ (reset) affects the entire card. It has the same effect as cycling power or a host **$$$** command. It is hard-wired, so it retains its function even if I2 is set to 1.

Handwheel Inputs

The handwheel inputs HWCA and HWCB can be connected to the second encoder counter on PMAC with jumpers E22 and E23. If these jumpers are on, nothing else should be connected to the Encoder 2 inputs. The signal can be interpreted either as quadrature or as pulse (HWCA) and direction (HWCB), depending on the value of I905. I905 also controls the direction sense of this input. Make sure that the Encoder 2 jumper E26 is set for single ended signals, connecting pins 1 and 2.

Optional Voltage to Frequency Converter

The WIPER analog input (0 to +10V on PMAC PCI referenced to digital ground) provides an input to a voltage-to-frequency converter (V/F) with a gain of 25 kHz/Volt, providing a range of 0-250 kHz. The output of the V/F can be connected to the Encoder 4 counter using jumpers E72 and E73. If these jumpers are on, nothing else should be connected to the Encoder 4 inputs. Make sure that the Encoder 4 jumper E24 is set for single-ended signals, connecting pins 1 and 2. This feature requires Option-15.

Frequency Decode

When used in this fashion, Encoder 4 must be set up for pulse-and-direction decode by setting I915 to 0 or 4. Usually, a value of 4 is used because with CHB4 (direction) unconnected, a positive voltage causes the counter to count up. The encoder conversion table can then take the difference in the counter each servo cycle and scale it, providing a value proportional to frequency, and therefore to the input voltage. Usually this is used for feedrate override (time base control), but the resulting value can be used for any purpose. The resulting value in the default setup can be found at X:$729,24

Power Supply

For the V/F converter to work, PMAC must have +/-12V supply referenced to digital ground. If PMAC is in a bus configuration, this usually comes through the bus connector from the bus power supply. In a standalone configuration, this supply must still be brought through the bus connector (or the supply terminal block), or it must be jumpered over from the analog side with E85, E87, and E88, defeating the optical isolation on the board.

Thumbwheel Multiplexer Port (JTHW Port)

The Thumbwheel Multiplexer Port, or Multiplexer Port, on the JTHW (J3) connector has eight input lines and eight output lines. The output lines can be used to multiplex large numbers of inputs and outputs on the port, and Delta Tau provides accessory boards and software structures (special M-variable definitions) to capitalize on this feature. Up to 32 of the multiplexed I/O boards may be daisy-chained on the port, in any combination.

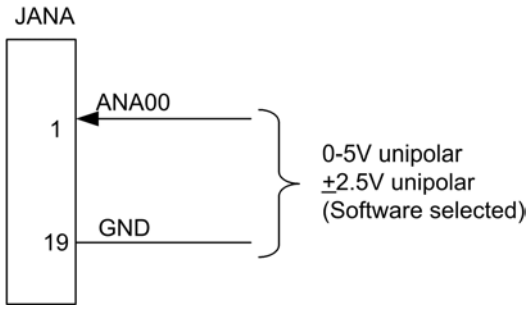
The ACC-18 Thumbwheel Multiplexer board provides up to 16 BCD thumbwheel digits or 64 discrete TTL inputs per board. The TWD and TWB forms of M-variables are used for this board. The Acc-34x family Serial I/O Multiplexer boards provides 64 I/O points per board, optically isolated from PMAC. The TWS form of M-variables is used for these boards. The Acc-8D Option 7 Resolver-to-Digital Converter board provides up to 4 resolver channels whose absolute positions can be read through the thumbwheel port. The TWR form of M-variables is used for this board. The Acc-8D Option 9 Yaskawa™ Absolute Encoder Interface board can connect to up to 4 of these encoders. The absolute position is read serially through the multiplexer port on power up.

If none of these accessory boards is used, the inputs and outputs on this port may be used as discrete, non-multiplexed I/O. They map into PMAC's processor space at Y address $78801. The suggested M-variable definitions for this use are M40 to M47 for the 8 outputs, and M50 to M57 for the eight inputs. The Acc-27 Optically Isolated I/O board buffers the I/O in this non-multiplexed form, with each point rated to 24V and 100 mA.

Optional Analog Inputs (JANA Port)

The JANA port is present only if Option 12 is ordered for the PMAC PCI. Option 12 provides eight 12-bit analog inputs (ANAI00-ANAI07). Option 12A provides eight additional 12-bit analog inputs (ANA08-ANAI15) for a total of 16 inputs. The analog inputs can be used as unipolar inputs in the 0V to +5V range, or bi-polar inputs in the -2.5V to +2.5V range.

The analog-to-digital converters on PMAC require +5V and -12V supplies. These supplies are not isolated from digital +5V circuitry on PMAC. If the PMAC is plugged into the PCI bus, these supplies are taken from the bus power supply. In a standalone application, these supplies must be brought in on terminal block TB1. The -12V and matching +12V supply voltages are available on the J30 connector to supply the analog circuitry providing the signals.



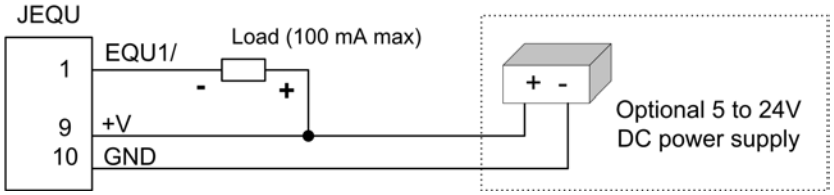
Only one pair of analog-to-digital converter registers is available to the PMAC processor at any given time. The data appears to the processor at address Y:$78808. The data from the selected analog input 0 to 7 (ANAI00-ANAI07) appears in the low 12-bits; the data from the selected analog input 8 to 15 (ANAI08-ANAI15) appears in the high 12-bits (this data is present only if Option 12A has been ordered). The input is selected and the conversion is started by writing to this same word address Y:$78808. A value of 0 to 7 written into the low 12-bits selects the analog input channel of that number (ANAI00-ANAI07) to be converted in unipolar mode (0V to +5V). A value of 0 to 7 written into the high 12-bits selects the analog input channel numbered eight greater (ANAI08-ANAI15) in unipolar mode. If the value written into either the low 12-bits or the high 12-bits is eight higher (8 to 15), the same input channel is selected, but the conversion is in bipolar mode (-2.5V to +2.5V).

Turbo PMAC variables I5060 to 5096 allow an automatic conversion of the analog inputs. The data can be read from registers Y:$3400 to Y:$341F by setting variables I5061 to I5076 to 8. See the Turbo PMAC Software Reference manual for further details.

Compare Equal Outputs Port (JEQU Port)

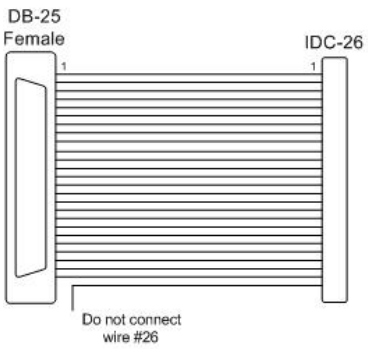
The compare-equals (EQU) outputs have a dedicated use of providing a signal edge when an encoder position reaches a pre-loaded value. This is useful for scanning and measurement applications. Instructions for use of these outputs are in the PMAC User Manual.

Outputs can be configured sinking or sourcing by replacing the chips U37 or U53 and configuring the jumpers E101-102 or E114-E115. The voltage levels can be configured individually by removing resistor packs RP43 or RP56 and connecting an external pull-up resistor in each output to the desired voltage level.



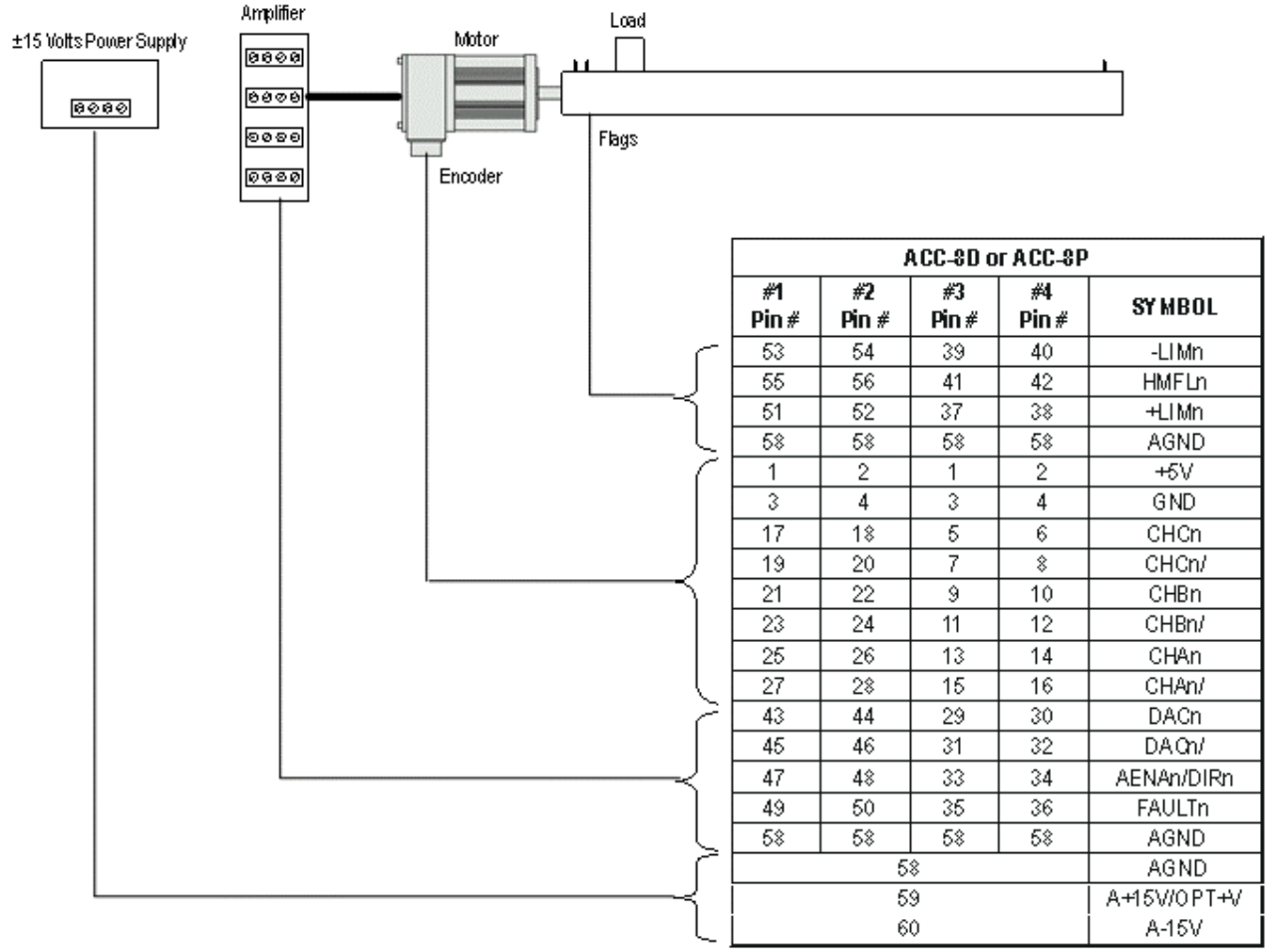
Serial Port (JRS422 Port)

For serial communications, use a serial cable to connect the PC's COM port to the PMAC's J4 serial port connector. Delta Tau provides the Acc-3D cable that connects the PMAC PCI to a DB-25 connector for this purpose. Standard DB-9-to-DB-25 or DB-25-to-DB-9 adapters may be needed for a particular setup. Jumper E110 selects between RS-232 or RS422 signals type for the J4 connector. If a cable must be made, the easiest approach is to use a flat cable prepared with flat-cable type connectors as indicated in the following diagram:

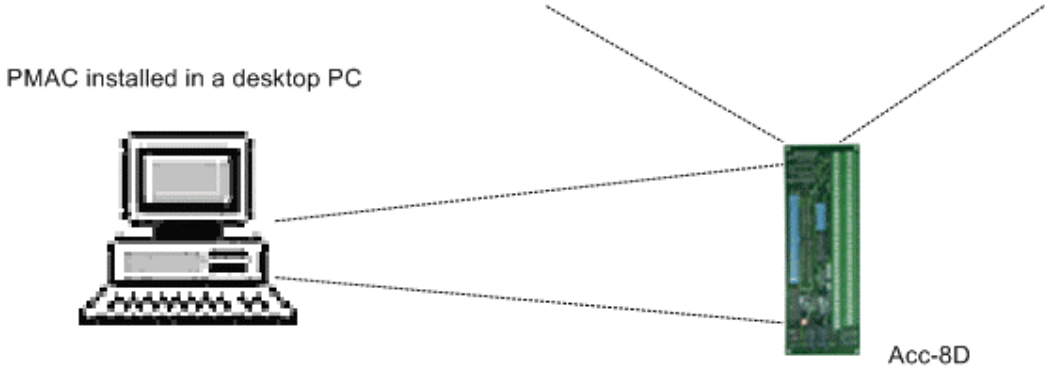


PMAC (IDC-26)	PC (DB-25)
1	1
2	14
3	2 (TXD)
4	15
5	3 (RXD)
6	16
7	4 (RTS)
8	17
9	5 (CTS)
10	18
11	6 (DSR)
12	19
13	7 (Gnd)
14	20 (DTR)
15	8
16	21
17	9
18	22
19	10
20	23
21	11
22	24
23	12
24	25
25	13
26	No connect

Machine Connections Example



ACC-8D or ACC-8P				
#1 Pin #	#2 Pin #	#3 Pin #	#4 Pin #	SYMBOL
53	54	39	40	-LIMn
55	56	41	42	HMFLn
51	52	37	38	+LIMn
58	58	58	58	AGND
1	2	1	2	+5V
3	4	3	4	GND
17	18	5	6	CHCn
19	20	7	8	CHCn/
21	22	9	10	CHBn
23	24	11	12	CHBn/
25	26	13	14	CHAn
27	28	15	16	CHAn/
43	44	29	30	DACn
45	46	31	32	DACn/
47	48	33	34	AENAn/DIRn
49	50	35	36	FAULTn
58	58	58	58	AGND
58				AGND
59				A+15V/OPT+V
60				A-15V



Note: For this configuration, jumpers E85, E87, E89, E90 and E100 are left at the default settings.

MATING CONNECTORS

This section lists several options for each connector. Choose an appropriate one for an application. (See the PMAC mating connector sketch for typical connection.)

Base Board Connectors

J1 (JDISP)/Display

- Two 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0, T&B Ansley P/N 609-1441
- 171-14 T&B Ansley standard flat cable stranded 14-wire
- Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1

J2 (JPAN)/Control Panel

- Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0, T&B Ansley P/N 609-2641
- 171.26.T&B Ansley standard flat cable stranded 26-wire
- Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J3 (JTHW)/Multiplexer Port

- Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0, T&B Ansley P/N 609-2641
- 171-26 T&B Ansley standard flat cable stranded 26-wire
- Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J4 (JRS422)/RS232 or 422/Serial Communications

- Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0, T&B Ansley P/N 609-2641
- 171-26 T&B Ansley standard flat cable stranded 26-wire
- Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J5 (JOPT)/OPTO I/O

- Two 34-pin female flat cable connector Delta Tau P/N 014-R00F34-0k0, T&B Ansley P/N 609-3441
- 171-34 T&B Ansley standard flat cable stranded 34-wire
- Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J6 (JXIO)/Expansion Board

- Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0, T&B Ansley P/N 609-1041
- 171-10 T&B Ansley standard flat cable stranded 10-wire
- Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J7 (JMACH2)/Second Machine Connector (Option 1 Required)

- Two 60-pin female flat cable connector Delta Tau P/N 014-R00F60-0K0, T&B Ansley P/N 609-6041 available as Acc-8P or 8D
- 171-60 T&B Ansley □tandard flat cable stranded 60-wire
- Phoenix varioface module type FLKM 60 (male pins) P/N 22 81 09 2

Note:

Normally, J7 and J8 are used with Acc-8P or 8D with Option P, which provides complete terminal strip fan-out of all connections.

J8 (JMACH1)/First Machine Connector

- Two 60-pin female flat cable connector Delta Tau P/N 014-R00F60-0K0, T&B Ansley P/N 609-6041 available as Acc-8P or 8D
- 171-60 T&B Ansley standard flat cable stranded 60-wire
- Phoenix varioface module type FLKM 60 (male pins) P/N 22 81 09 2

Note:

Normally, J7 and J8 are used with Acc-8P or 8D with Option P, which provides complete terminal strip fan-out of all connections.

JS1/A-D Inputs 1-4

- Two 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0, T&B Ansley P/N 609-1641
- 171-16 T&B Ansley standard flat cable stranded 16-wire
- Phoenix varioface module type FLKM 16 (male pins) P/N 22 81 03 4

JS2/A-D Inputs 5-8 (Option 1 Required)

- Two 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0, T&B Ansley P/N 609-1641
- 171-16 T&B Ansley standard flat cable stranded 16-wire
- Phoenix varioface module type FLKM 16 (male pins) P/N 22 81 03 4

JEQU/Position Compare

- Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0, T&B Ansley P/N 609-1041
- 171-10 T&B Ansley standard flat cable stranded 10-wire
- Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

JANA/Analog Inputs Option

- Two 20-pin female flat cable connector Delta Tau P/N 014-R00F20-0K0, T&B Ansley P/N 609-2041
- 171-20 T&B Ansley standard flat cable stranded 20-wire
- Phoenix varioface modules type FLKM20 (male pins)

CPU Board Connectors

J2 (JEXP)/Expansion

- Two 50-pin female flat cable connector Delta Tau P/N 014-R00F50-0K0, T&B Ansley P/N 609-5041
- 171-50 T&B Ansley standard flat cable stranded 50-wire
- Phoenix varioface module type FLKM 50 (male pins) P/N 22 81 08 9

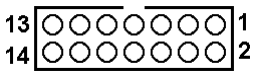
J8 (JAUX232)/Auxiliary RS232

- Two 10-pin female flat cable connector Delta Tau P/N 014-ROOF10-0K0, T&B Ansley P/N 609-1041
- 171-10 T&B Ansley standard flat cable stranded 10-wire
- Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

BASE BOARD CONNECTOR PINOUTS

J1: Display Port Connector

J1 JDISP (14-Pin Connector)



Pin #	Symbol	Function	Description	Notes
1	Vdd	Output	+5V Power	Power supply out
2	Vss	Common	PMAC Common	
3	Rs	Output	Read Strobe	TTL signal out
4	Vee	Output	Contrast Adjust. VEE	0 to +5 VDC *
5	E	Output	Display Enable	High is enable
6	R/W	Output	Read or Write	TTL signal out
7	DB1	Output	Display Data1	
8	DB0	Output	Display Data0	
9	DB3	Output	Display Data3	
10	DB2	Output	Display Data2	
11	DB5	Output	Display Data5	
12	DB4	Output	Display Data4	
13	DB7	Output	Display Data7	
14	DB6	Output	Display Data6	

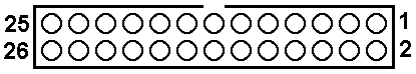
The JDISP connector is used to drive the 2-line x 24-character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (Acc 12C) display unit. The **DISPLAY** command may be used to send messages and values to the display.

* **Note**: Controlled by potentiometer R1.

See Also:

Program Commands: **DISPLAY**
Accessories: Acc-12, 12A, 12C, Acc-16D
Memory Map: Y:$0780 - $07D1

J2: Control Panel Port Connector

J2 JPAN (26-Pin Connector)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	+5V	Output	+5V Power	For remote panel
2	GND	Common	PMAC Common	
3	FPD0/	Input	Motor/C.S. Select Bit 0	Low is TRUE
4	JOG-/	Input	C - C.	Low is JOG -
5	FPD1/	Input	Motor /C.S. Select Bit 1	Low is TRUE
6	JOG+/	Input	V + V.	Low is JOG +
7	PREJ/	Input	Return to Prejog Position	Low is RETURN Equiv to J= CMD
8	STRT/	Input	Start Program Run	Low is START Equiv to R CMD
9	STEP/	Input	Step Through Program	Low is STEP Equiv to S OR Q
10	STOP/	Input	Stop Program Run	Low is STOP Equiv to A
11	HOME/	Input	Home Search Command	Low is GO HOME Equiv to HM
12	HOLD/	Input	Hold Motion	Low is HOLD Equiv to H
13	FPD2/	Input	Motor /C.S. Select Bit 2	Low is TRUE
14	FPD3/	Input	Motor /C.S. Select Bit 3	Low is TRUE
15	INIT/	Input	Reset PMAC	Low is RESET Equiv to $$$
16	HWCA	Input	Handwheel Encoder A Channel	5V TTL sq. pulse must use E23 (CHA2)
17	IPLD/	Output	In Position Ind. (C.S.)	Low lights LED
18	BRLD/	Output	Buffer Request Ind.	Low lights LED
19	ERLD/	Output	Fatal Follow Err (C.S.)	Low lights LED
20	WIPER	Input	Feed Pot Wiper	0 to +10V input must use E72, E73 (CHA4)
21	(SPARE)	N.C.		
22	HWCB	Input	Handwheel Encoder B Channel	5V TTL SQ. pulse must use E22 (CHB2)
23	F1LD/	Output	Warn Follow Err (C.S.)	Low lights LED
24	F2LD/	Output	Watchdog Timer	Low lights LED
25	+5V	Output	+5V Power	For remote panel
26	GND	Common	PMAC Common	

The JPAN connector can be used to connect the Acc-16 (Control Panel), or customer-provided I/O, to the PMAC, providing manual control of PMAC functions via simple toggle switches. If the automatic control panel input functions are disabled (I2=1), the inputs become general-purpose TTL inputs, and the coordinate system (C.S.) specific outputs pertain to the host-addressed coordinate system.

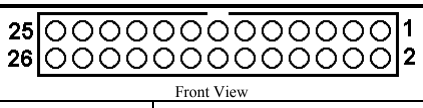
See Also:

Control panel inputs, Accessories: Acc-16, Acc-39

I-variables: I2, Ix06. I/O and Memory Map: Y:$78800. Suggested M-variables M20 - M32

J3: Multiplexer Port Connector

J3 JTHW (26-Pin Connector)



Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Input	Data-0 Input	Data input from multiplexed accessory
4	SEL0	Output	Select-0 Output	Multiplexer select output
5	DAT1	Input	Data-1 Input	Data input from multiplexed accessory
6	SEL1	Output	Select-1 Output	Multiplexer select output
7	DAT2	Input	Data-2 Input	Data input from multiplexed accessory
8	SEL2	Output	Select-2 Output	Multiplexer select output
9	DAT3	Input	Data-3 Input	Data input from multiplexed accessory
10	SEL3	Output	Select-3 Output	Multiplexer select output
11	DAT4	Input	Data-4 Input	Data input from multiplexed accessory
12	SEL4	Output	Select-4 Output	Multiplexer select output
13	DAT5	Input	Data-5 Input	Data input from multiplexed accessory
14	SEL5	Output	Select-5 Output	Multiplexer select output
15	DAT6	Input	Data-6 Input	Data input from multiplexed accessory
16	SEL6	Output	Select-6 Output	Multiplexer select output
17	DAT7	Input	Data-7 Input	Data input from multiplexed accessory
18	SEL7	Output	Select-7 Output	Multiplexer select output
19	N.C.	N.C.	No Connection	
20	GND	Common	PMAC Common	
21	BRLD/	Output	Buffer Request	Low is Buffer Request
22	GND	Common	PMAC Common	
23	IPLD/	Output	In Position	Low is In Position
24	GND	Common	PMAC Common	
25	+5V	Output	+5VDC Supply	Power supply out
26	INIT/	Input	PMAC Reset	Low is Reset

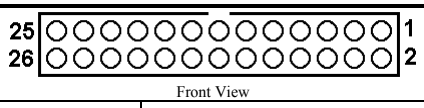
The JTHW multiplexer port provides eight inputs and eight outputs at TTL levels. While these I/O can be used in un-multiplexed form for 16 discrete I/O points, most will utilize PMAC software and accessories to use this port in multiplexed form to greatly multiply the number of I/O that can be accessed on this port. In multiplexed form, some of the SELn outputs are used to select which of the multiplexed I/O are to be accessed.

See also:

I/O and Memory Map Y:$78801
Suggested M-variables M40 - M58
M-variable formats TWB, TWD, TWR, TWS
Acc-8D Opt 7, Acc-8D Opt 9, Acc-18, Acc-34x, NC Control Panel

J4: Serial Port Connector

J4 JRS422 (26-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	CHASSI	Common	PMAC Common	
2	S+5V	Output	+5VDC Supply	Deactivated by E8
3	RD-	Input	Receive Data	Diff. I/O low TRUE **
4	RD+	Input	Receive Data	Diff. I/O high TRUE *
5	SD-	Output	Send Data	Diff. I/O low TRUE **
6	SD+	Output	Send Data	Diff. I/O high TRUE *
7	CS+	Input	Clear to Send	Diff. I/O high TRUE **
8	CS-	Input	Clear to Send	Diff. I/O low TRUE *
9	RS+	Output	Request to Send	Diff. I/O high TRUE **
10	RS-	Output	Request to Send	Diff. I/O low TRUE *
11	DTR	Bidirect	Data Terminal Ready	TIED TO DSR
12	INIT/	Input	PMAC Reset	Low is RESET
13	GND	Common	PMAC Common	**
14	DSR	Bidirect	Data Set Ready	Tied to DTR
15	SDIO-	Bidirect	Special Data	Diff. I/O low TRUE
16	SDIO+	Bidirect	Special Data	Diff. I/O high TRUE
17	SCIO-	Bidirect	Special Control	Diff. I/O low TRUE
18	SCIO+	Bidirect	Special Control	Diff. I/O high TRUE
19	SCK-	Bidirect	Special Clock	Diff. I/O low TRUE
20	SCK+	Bidirect	Special Clock	Diff. I/O high TRUE
21	SERVO-	Bidirect	Servo Clock	Diff. I/O low TRUE ***
22	SERVO+	Bidirect	Servo Clock	Diff. I/O high TRUE ***
23	PHASE-	Bidirect	Phase Clock	Diff. I/O low TRUE ***
24	PHASE+	Bidirect	Phase Clock	Diff. I/O high TRUE ***
25	GND	Common	PMAC Common	
26	+5V	Output	+5VDC Supply	Power supply out

The JRS422 connector provides the PMAC with the ability to communicate both in RS422 and RS232. In addition, this connector is used to daisy chain interconnect multiple PMACs for synchronized operation.

Jumper E110 selects between RS-232 or RS-422 signal types.

Jumper E110 enables or disables the use of the Phase, Servo and Init lines

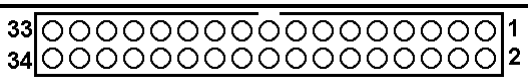
* **Note:** Required for communications to an RS-422 host port

** **Note:** Required for communications to an RS-422 or RS-232 host port

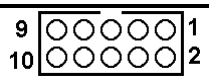
*** **Note:** Output on card @0; input on other cards. These pins are for synchronizing multiple PMACs together by sharing their phasing and servo clocks. The PMAC designated as card 0 (@0) by its jumpers E40-E43 outputs its clock signals. Other PMACs designated as cards 1-15 (@1-@F) by their jumpers E40-E43 take these signals as inputs. If synchronization is desired, these lines should be connected even if serial communications is not used.

See Also:
Serial Communications
Synchronizing PMAC to other PMACs

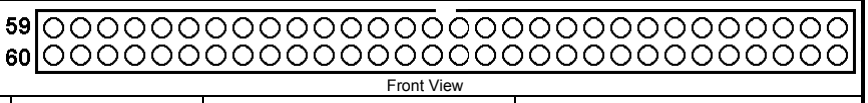
J5: I/O Port Connector

J5 JOPT (34-Pin Connector)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	MI8	Input	Machine Input 8	Low is TRUE
2	GND	Common	PMAC Common	
3	MI7	Input	Machine Input 7	Low is TRUE
4	GND	Common	PMAC Common	
5	MI6	Input	Machine Input 6	Low is TRUE
6	GND	Common	PMAC Common	
7	MI5	Input	Machine Input 5	Low is TRUE
8	GND	Common	PMAC Common	
9	MI4	Input	Machine Input 4	Low is TRUE
10	GND	Common	PMAC Common	
11	MI3	Input	Machine Input 3	Low is TRUE
12	GND	Common	PMAC Common	
13	MI2	Input	Machine Input 2	Low is TRUE
14	GND	Common	PMAC Common	
15	MI1	Input	Machine Input 1	Low is TRUE
16	GND	Common	PMAC Common	
17	MO8	Output	Machine Output 8	Low-True (Sinking); High-True (Sourcing)
18	GND	Common	PMAC Common	
19	MO7	Output	Machine Output 7	" "
20	GND	Common	PMAC Common	
21	MO6	Output	Machine Output 6	" "
22	GND	Common	PMAC Common	
23	MO5	Output	Machine Output 5	" "
24	GND	Common	PMAC Common	
25	MO4	Output	Machine Output 4	" "
26	GND	Common	PMAC Common	
27	MO3	Output	Machine Output 3	" "
28	GND	Common	PMAC Common	
29	MO2	Output	Machine Output 2	" "
30	GND	Common	PMAC Common	
31	MO1	Output	Machine Output 1	" "
32	GND	Common	PMAC Common	
33	+V	Input/Output	+V Power I/O	+V = +5V to +24V +5V out from PMAC, +5 to +24V in from external source, diode isolation from PMAC
34	GND	Common	PMAC Common	
This connector provides means for eight general-purpose inputs and eight general-purpose outputs. Inputs and outputs may be configured to accept or provide either +5V or +24V signals. Outputs can be made sourcing with an IC (U13 to UDN2981) and jumper (E1 and E2) change. E7 controls whether the inputs are pulled up or down internally. Outputs are rated at 100mA per channel.				

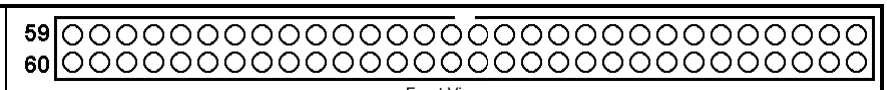
J6: Auxiliary I/O Port Connector

J6 JXIO (10-Pin Connector)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	CHA1	Input	Encoder A Chan. Pos.	Axis #1 for resolver
2	CHB1	Input	Encoder B Chan. Pos.	Axis #1 for resolver
3	CHC1	Input	Encoder C Chan. Pos.	Axis #1 for resolver
4	CHA3	Input	Encoder A Chan. Pos.	Axis #3 for resolver
5	CHB3	Input	Encoder B Chan. Pos.	Axis #3 for resolver
6	CHC3	Input	Encoder C Chan. Pos.	Axis #3 for resolver
7	E63	Input	Interrupt IR4	Interrupt from exp brd
8	E59	Input	Interrupt IR5	Interrupt from exp brd
9	SCLK	Output	Encoder Clock	Encoder sample rate
10	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for all channels
This connector is used for miscellaneous I/O functions related to expansion cards that are used with PMAC.				

J7: Machine Port 2 Connector

J7 JMACH2 (60-Pin Header)				
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	+5V	Output	+5V Power	For encoders, 1
2	+5V	Output	+5V Power	For encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC7	Input	Encoder C Ch. Pos.	2
6	CHC8	Input	Encoder C Ch. Pos.	2
7	CHC7/	Input	Encoder C Ch. Neg.	2,3
8	CHC8/	Input	Encoder C Ch. Neg.	2,3
9	CHB7	Input	Encoder B Ch. Pos.	2
10	CHB8	Input	Encoder B Ch. Pos.	2
11	CHB7/	Input	Encoder B Ch. Neg.	2,3
12	CHB8/	Input	Encoder B Ch. Neg.	2,3
13	CHA7	Input	Encoder A Ch. Pos.	2
14	CHA8	Input	Encoder A Ch. Pos.	2
15	CHA7/	Input	Encoder A Ch. Neg.	2,3
16	CHA8/	Input	Encoder A Ch. Neg.	2,3
17	CHC5	Input	Encoder C Ch. Pos.	2
18	CHC6	Input	Encoder C Ch. Pos.	2
19	CHC5/	Input	Encoder C Ch. Neg.	2,3
20	CHC6/	Input	Encoder C Ch. Neg.	2,3
21	CHB5	Input	Encoder B Ch. Pos.	2
22	CHB6	Input	Encoder B Ch. Pos.	2
23	CHB5/	Input	Encoder B Ch. Neg.	2,3
24	CHB6/	Input	Encoder B Ch. Neg.	2,3
25	CHA5	Input	Encoder A Ch. Pos.	2
26	CHA6	Input	Encoder A Ch. Pos.	2
27	CHA5/	Input	Encoder A Ch. Neg.	2,3
28	CHA6/	Input	Encoder A Ch. Neg.	2,3
29	DAC7	Output	Analog Out Pos. 7	4
30	DAC8	Output	Analog Out Pos. 8	4
31	DAC7/	Output	Analog Out Neg. 7	4,5
32	DAC8/	Output	Analog Out Neg. 8	4,5
33	AENA7/DIR7	Output	Amp-Ena/Dir. 7	6
34	AENA8/DIR8	Output	Amp-Ena/Dir. 8	6
35	FAULT7	Input	Amp-Fault 7	7
36	FAULT8	Input	Amp-Fault 8	7
37	+LIM7	Input	Neg. End Limit 7	8,9
38	+LIM8	Input	Neg. End Limit 8	8,9
39	-LIM7	Input	Pos. End Limit 7	8,9

J7 JMACH2 (60-Pin Header) (Continued)



Pin #	Symbol	Function	Description	Notes
40	-LIM8	Input	Pos. End Limit 8	8,9
41	HMFL7	Input	Home Flag 7	10
42	HMFL8	Input	Home Flag 8	10
43	DAC5	Output	Analog Out Pos. 5	4
44	DAC6	Output	Analog Out Pos. 6	4
45	DAC5/	Output	Analog Out Neg. 5	4,5
46	DAC6/	Output	Analog Out Neg. 6	4,5
47	AENA5/DIR5	Output	Amp. Ena/.Dir. 5	6
48	AENA6/DIR6	Output	Amp. Ena/.Dir. 6	6
49	FAULT5	Input	Amp Fault 5	7
50	FAULT6	Input	Amp Fault 6	7
51	+LIM5	Input	Neg. End Limit 5	8,9
52	+LIM6	Input	Neg. End Limit 6	8,9
53	-LIM5	Input	Pos. End Limit 5	8,9
54	-LIM6	Input	Pos. End Limit 6	8,9
55	HMFL5	Input	Home Flag 5	10
56	HMFL6	Input	Home Flag 6	10
57	ORST/	Output	Reset Signal	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15V/Flag Supply	
60	A-15V	Input	Analog -15V/Flag Supply	

The J7 connector is used to connect the PMAC to the second four channels (Channels 5, 6, 7, and 8) of servo amps, flags, and encoders.

Note 1: In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on your version of PMAC, it is preferable to bring the +5V power in through the terminal block.

Note 2: Referenced to digital common (GND). Maximum of ± 12V permitted between this signal and its complement.

Note 3: Leave this input floating if not used (i.e. digital single-ended encoders). In this case, jumper (E18 - 21, E24 - 27) for channel should hold input at 2.5V.

Note 4: ± 10V, 10mA max, referenced to analog common (AGND).

Note 5: Leave floating if not used; do not tie to AGND. In this case AGND is the return line.

Note 6: Functional polarity controlled by jumper(s) E17. Choice between AENA and DIR use controlled by Ix02 and Ix25.

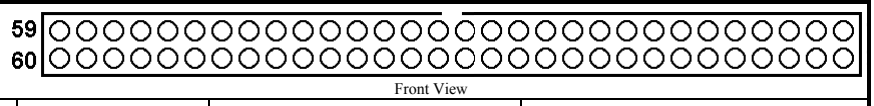
Note 7: Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software. Automatic fault function can be disabled with Ix25.

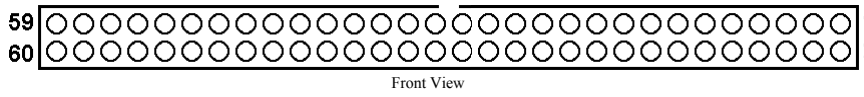
Note 8: Pins marked *-LIMn* should be connected to switches at the *positive* end of travel. Pins marked *+LIMn* should be connected to switches at the *negative* end of travel.

Note 9: Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

Note 10: Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a 0 in PMAC software.

J8: Machine Port 1 Connector

J8 JMACH1 (60-Pin Header)	 Front View			
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	+5V	Output	+5V Power	For encoders, 1
2	+5V	Output	+5V Power	For encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC3	Input	Encoder C Chan. Pos.	2
6	CHC4	Input	Encoder C Chan. Pos.	2
7	CHC3/	Input	Encoder C Chan. Neg.	2,3
8	CHC4/	Input	Encoder C Chan. Neg.	2,3
9	CHB3	Input	Encoder B Chan. Pos.	2
10	CHB4	Input	Encoder B Chan. Pos.	2
11	CHB3/	Input	Encoder B Chan. Neg.	2,3
12	CHB4/	Input	Encoder B Chan. Neg.	2,3
13	CHA3	Input	Encoder A Chan. Pos.	2
14	CHA4	Input	Encoder A Chan. Pos.	2
15	CHA3/	Input	Encoder A Chan. Neg.	2,3
16	CHA4/	Input	Encoder A Chan. Neg.	2,3
17	CHC1	Input	Encoder C Chan. Pos.	2
18	CHC2	Input	Encoder C Chan. Pos.	2
19	CHC1/	Input	Encoder C Chan. Neg.	2,3
20	CHC2/	Input	Encoder C Chan. Neg.	2,3
21	CHB1	Input	Encoder B Chan. Pos.	2
22	CHB2	Input	Encoder B Chan. Pos.	2
23	CHB1/	Input	Encoder B Chan. Neg.	2,3
24	CHB2/	Input	Encoder B Chan. Neg.	2,3
25	CHA1	Input	Encoder A Chan. Pos.	2
26	CHA2	Input	Encoder A Chan. Pos.	2
27	CHA1/	Input	Encoder A Chan. Neg.	2,3
28	CHA2/	Input	Encoder A Chan. Neg.	2,3
29	DAC3	Output	Analog Out Pos. 3	4
30	DAC4	Output	Analog Out Pos. 4	4
31	DAC3/	Output	Analog Out Neg. 3	4,5
32	DAC4/	Output	Analog Out Neg. 4	4,5
33	AENA3/DIR3	Output	Amp. Ena/Dir. 3	6
34	AENA4/DIR4	Output	Amp. Ena/. 4	6
35	FAULT3	Input	Amp Fault 3	7
36	FAULT4	Input	Amp Fault 4	7
37	+LIM3	Input	Neg. End Limit 3	8,9
38	+LIM4	Input	Neg. End Limit 4	8,9
39	-LIM3	Input	Pos. End Limit 3	8,9

J8 JMACH1 (60-Pin Header) (Continued)	 Front View

Pin #	Symbol	Function	Description	Notes
40	-LIM4	Input	Pos. End Limit 4	8,9
41	HMFL3	Input	Home Flag 3	10
42	HMFL4	Input	Home Flag 4	10
43	DAC1	Output	Analog Out Pos. 1	4
44	DAC2	Output	Analog Out Pos. 2	4
45	DAC1/	Output	Analog Out Neg. 1	4,5
46	DAC2/	Output	Analog Out Neg. 2	4,5
47	AENA1/DIR1	Output	Amp/Ena/Dir. 1	6
48	AENA2/DIR2	Output	Amp/Ena/Dir. 2	6
49	FAULT1	Input	Amp Fault1	7
50	FAULT2	Input	Amp Fault1 2	7
51	+LIM1	Input	Neg. End Limit 1	8,9
52	+LIM2	Input	Neg. End Limit 2	8,9
53	-LIM1	Input	Pos. End Limit 1	8,9
54	-LIM2	Input	Pos. End Limit 2	8,9
55	HMFL1	Input	Home Flag 1	10
56	HMFL2	Input	Home Flag 2	10
57	FEFCO/	Output	FE/Watchdog Out	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15V Supply	

The J8 connector is used to connect PMAC to the first four channels (Channels 1, 2, 3, and 4) of servo amps, flags, and encoders.

Note 1: In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on your version of PMAC, it is preferable to bring the +5V power in through the terminal block.

Note 2: Referenced to digital common (GND). Maximum of ± 12V permitted between this signal and its complement.

Note 3: Leave this input floating if not used (i.e. digital single-ended encoders). In this case, jumper (E18 - 21, E24 - 27) for channel should hold input at 2.5V.

Note 4: ± 10V, 10mA max, referenced to analog common (AGND).

Note 5: Leave floating if not used; do not tie to AGND. In this case AGND is the return line.

Note 6: Functional polarity controlled by jumper(s) E17. Choice between AENA and DIR use controlled by Ix02 and Ix25.

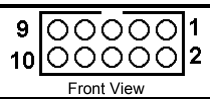
Note 7: Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software. Automatic fault function can be disabled with Ix25.

Note 8: Pins marked *-LIMn* should be connected to switches at the *positive* end of travel. Pins marked *+LIMn* should be connected to switches at the *negative* end of travel.

Note 9: Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

Note 10: Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software.

J9 (JEQU): Position-Compare Connector

J9 JEQU (10-Pin Connector)				
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	EQU1/	Output	Encoder 1 Comp-EQ	Low is TRUE
2	EQU2/	Output	Encoder 2 Comp -EQ	Low is TRUE
3	EQU3/	Output	Encoder 3 Comp -EQ	Low is TRUE
4	EQU4/	Output	Encoder 4 Comp -EQ	Low is TRUE
5	EQU5/	Output	Amp Enable 1	Low is TRUE
6	EQU6/	Output	Amp Enable 2	Low is TRUE
7	EQU7/	Output	Amp Enable 3	Low is TRUE
8	EQU8/	Output	Amp Enable 4	Low is TRUE
9	A+V	Supply	Positive Supply	+5V to +24V
10	AGND	Common	Analog Ground	
This connector provides the position-compare outputs and the amplifier enable outputs for the four servo interface channels. The board is shipped by default with a ULN2803A or equivalent open-collector driver IC on U37 and U53. It may be replaced with UDN2891A or equivalent open-emitter driver (E101-E102 or E114-E115 must be changed!), or a 74ACT563 or equivalent 5V CMOS driver.				

J30 (JANA) Analog Input Port Connector (Optional)

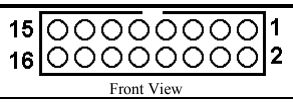
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	ANAI00	Input	Analog Input 0	0-5V or +/-2.5V range
2	ANAI01	Input	Analog Input 1	0-5V or +/-2.5V range
3	ANAI02	Input	Analog Input 2	0-5V or +/-2.5V range
4	ANAI03	Input	Analog Input 3	0-5V or +/-2.5V range
5	ANAI04	Input	Analog Input 4	0-5V or +/-2.5V range
6	ANAI05	Input	Analog Input 5	0-5V or +/-2.5V range
7	ANAI06	Input	Analog Input 6	0-5V or +/-2.5V range
8	ANAI07	Input	Analog Input 7	0-5V or +/-2.5V range
9	ANAI08	Input	Analog Input 8	0-5V or +/-2.5V range *
10	ANAI09	Input	Analog Input 9	0-5V or +/-2.5V range *
11	ANAI10	Input	Analog Input 10	0-5V or +/-2.5V range *
12	ANAI11	Input	Analog Input 11	0-5V or +/-2.5V range *
13	ANAI12	Input	Analog Input 12	0-5V or +/-2.5V range *
14	ANAI13	Input	Analog Input 13	0-5V or +/-2.5V range *
15	ANAI14	Input	Analog Input 14	0-5V or +/-2.5V range *
16	ANAI15	Input	Analog Input 15	0-5V or +/-2.5V range *
17	GND	Common	PMAC Common	Not isolated from digital
18	+12V	Output	Pos. Supply Volt.	To power ext. circuitry
19	GND	Common	PMAC Common	Not isolated from digital
20	-12V	Output	Neg. Supply Volt.	To power ext circuitry
The JANA connector provides the inputs for the 8 or 16 optional analog inputs on the PMAC2. * Only present if Option-12 ordered.				

J31 (JUSB) Universal Serial Bus Port (Optional)

Pin #	Symbol	Function
1	VCC	N.C.
2	D-	Data-
3	D+	Data+
4	GND	GND
5	SHELL	Shield
6	SHELL	Shield

JS1: A/D Port 1 Connector

JS1 (16-Pin Header)

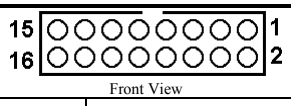


Front View

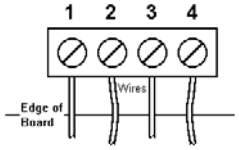
Pin #	Symbol	Function	Description	Notes
1	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for Chan. 1, 2, 3, 4
2	BDATA1	Output	D to A Data	DAC data for Chan. 1, 2, 3, 4
3	ASEL0/	Output	Chan. Select Bit 0	Select for Chan. 1, 2, 3, 4
4	ASEL1/	Output	Chan. Select Bit 1	Select for Chan. 1, 2, 3, 4
5	CNVRT01	Output	A to D Convert	ADC convert sig. Chan. 1, 2, 3, 4
6	ADCIN1	Input	A to D Data	ADC data for Chan. 1, 2, 3, 4
7	OUT1/	Output	Amp Enable/Dir	Amp Enable/Dir. For Chan. 1
8	OUT2/	Output	Amp Enable/Dir	Amp Enable/Dir. For Chan. 2
9	OUT3/	Output	Amp Enable/Dir	Amp Enable/Dir. For Chan. 3
10	OUT4/	Output	Amp Enable/Dir	Amp Enable/Dir. For Chan. 4
11	HF41	Input	Amp Fault	Amp fault input for Chan. 1
12	HF42	Input	Amp Fault	Amp fault input for Chan. 2
13	HF43	Input	Amp Fault	Amp fault input for Chan. 3
14	HF44	Input	Amp Fault	Amp fault input for Chan. 4
15	+5V	Output	+5V Supply	Power supply out
16	GND	Common	PMAC Common	

Acc-28A/B connection; digital amplifier connection.

JS2: A/D Port 2 Connector

JS2 (16-Pin Header)			 Front View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for Chan. 5, 6, 7, 8
2	BDATA2	Output	D to A Data	DAC data for Chan. 5, 6, 7, 8
3	ASEL2/	Output	Chan. Select Bit 2	Select for Chan. 5, 6, 7, 8
4	ASEL3/	Output	Chan. Select Bit 3	Select for Chan. 5, 6, 7, 8
5	CNVRT23	Output	A to D Convert	ADC convert sig Chan. 5, 6, 7, 8
6	ADCIN2	Input	A to D Data	ADC data for Chan. 5, 6, 7, 8
7	OUT5/	Output	Amp Enable/Dir	AMP enable/dir for Chan. 5
8	OUT6/	Output	Amp Enable/Dir	AMP enable/dir for Chan. 6
9	OUT7/	Output	Amp Enable/Dir	AMP enable/dir for Chan. 7
10	OUT8/	Output	Amp Enable/Dir	AMP enable/dir for Chan. 8
11	HF45	Input	Amp Fault	AMP fault input for Chan. 5
12	HF46	Input	Amp Fault	AMP fault input for Chan. 6
13	HF47	Input	Amp Fault	AMP fault input for Chan. 7
14	HF48	Input	Amp Fault	AMP fault input for Chan. 8
15	+5V	Output	+5V Supply	Power supply out
16	GND	Common	PMAC Common	
ACC-28A/B connection; digital amplifier connection.				

TB1 (JPWR)

TB1 (4-Pin Terminal Block)			 Top View	
Pin #	**Symbol**	**Function**	**Description**	**Notes**
1	GND	Common	Digital Ground	
2	+5V	Input	+5V Supply	Reference to digital ground
3	+12V	Input	+12V TO +15V Supply	Reference to digital ground
4	-12V	Input	-12V TO -15V Supply	Reference to digital ground
This terminal block may be used as an alternative power supply connector if PMAC PCI is not installed in a PC bus. The +5V powers the digital electronics. The +12V and -12V, if jumpers E85, E87, and E88 are installed, power the analog output stage (this defeats the optical isolation on PMAC). To keep the optical isolation between the digital and analog circuits on PMAC, provide analog power (+/-12V to +/-15V and AGND) through the JMACH connector, instead of the bus connector or this terminal block.				

SOFTWARE SETUP

Communications

Delta Tau provides communication tools that take advantage of the PCI bus Plug & Play feature of 32-bits Windows© based computers. Starting with MOTIONEXE.EXE version 10.32.00, which is included in PEWIN32 version 2.32 and newer, a PMAC2 PCI board plugged in a PCI bus slot will be recognized by the operating system when the computer is booted up. The available PCI address, dual-ported RAM address and Interrupt lines are set automatically by the operating system and can be checked (but not modified) in the MOTIONEXE.EXE application or the resources page of the device manager.

PMAC I-Variables

PMAC has a large set of Initialization parameters (I-variables) that determine the personality of the card for a specific application. Many of these are used to configure a motor. Once set up, these variables may be stored in non-volatile EAROM memory (using the **SAVE** command) so the card is always configured properly (PMAC loads the EAROM I-variable values into RAM on power-up).

The easiest way to program, set up and troubleshoot PMAC is by using the PMAC Executive Program PEWIN and its related add-on packages Turbo Setup and PMAC Plot. These software packages are available from Delta Tau, ordered through the Acc-9WN accessory.

The programming features and configuration variables for the PMAC PCI are discussed in the Turbo PMAC User and Software manuals.